INTEGRATED CIRCUITS

# DATA SHEET

# SAA7824

## CD audio decoder, digital servo and filterless DAC with integrated pre-amp and laser control (PhonIC)

Product specification Supersedes data of 2003 Aug 07 | 2003 Oct 01

Philips Semiconductors

PHILIPS

CONTENTS

## 1 FEATURES

- Decoder and servo parts are based upon the SAA732X design (the original features are maintained)
- Software compatibility is maintained with the SAA732X by using a similar register structure (new features are controlled from new shadow registers)
- 1×, 2× and 4× speed
- LF (servo) signals converted to digital representations by 6 oversampling bitstream ADCs
- HF part summed from signals D1 to D4 and converted into a digital signal by a data slicer
- On-chip buffering and filtering of the diode signals from the mechanism for signal optimization
- Selectable DC offset cancellation of quiescent mechanism voltages and dark currents
- On-chip laser power control (up to 120 mA)
- Laser on/off control, including ‘soft’ start control (zero to nominal power in 1 ms)
- Monitor control and feedback circuit to maintain nominal output power throughout laser life
- Dynamic element matching DAC with minimum external components
- DAC performance of –80 dB Total Harmonic Distortion + Noise (THD + N) and 90 dB Signal-to-Noise Ratio (S/N) A-weighted
- Separate left and right channel digital silence detection available on the KILL pins
- Digital silence detection on internal data and loopback (external) data
- 5 versatile pins, 2 inputs and 3 outputs
- Integrated CD text decoder with separate microcontroller interface
- Dedicated 4 MHz or 12 MHz clock output for microcontroller (configurable)
- Configured for N-sub monitor diode
- On-chip clock multiplier allows the use of an 8.4672 MHz crystal or ceramic resonator
- The M1 version has an EBU mute function which allows independent muting of data being transmitted over the EBU interface whilst maintaining the SPDIF frame structure.

## 2 GENERAL DESCRIPTION

This document covers versions M0 and M1 of the CD audio decoder IC.

The SAA7824 is a CD audio decoder IC which combines the function of the SAA732X IC with the pre-amplifier and laser control functions previously found in the TZA102X IC. The design is intended to reduce the external component count and hence the Bill Of Material (BOM).

Supply of this Compact Disc IC does not convey an implied license under any patent right to use this IC in any Compact Disc application.

## 3 ORDERING INFORMATION

| TYPE NUMBER | PACKAGE | | |
|---|---|---|---|
| | NAME | DESCRIPTION | VERSION |
| SAA7824HL | LQFP80 | plastic low profile quad flat package; 80 leads; body 12 × 12 × 1.4 mm | SOT315-1 |

## 4 QUICK REFERENCE DATA

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $V_{DDD}$ | digital supply voltage | | 1.65 | 1.8 | 1.95 | V |
| $V_{DDA}$ | analog supply voltage | | 3.0 | 3.3 | 3.6 | V |
| $I_{DD(tot)}$ | total supply current | n = 1 mode | – | 38 | – | mA |
| | | n = 2 mode | – | 39 | – | mA |
| | | n = 4 mode | – | 40 | – | mA |
| $f_{xtal}$ | crystal frequency | | – | 8.4672 | – | MHz |
| $T_{amb}$ | ambient temperature | | 0 | – | 70 | °C |
| $T_{stg}$ | storage temperature | | –55 | – | +125 | °C |
| $S/N_{DAC}$ | onboard DAC signal-to-noise ratio | | – | 90 | – | dB |

## 5 BLOCK DIAGRAM

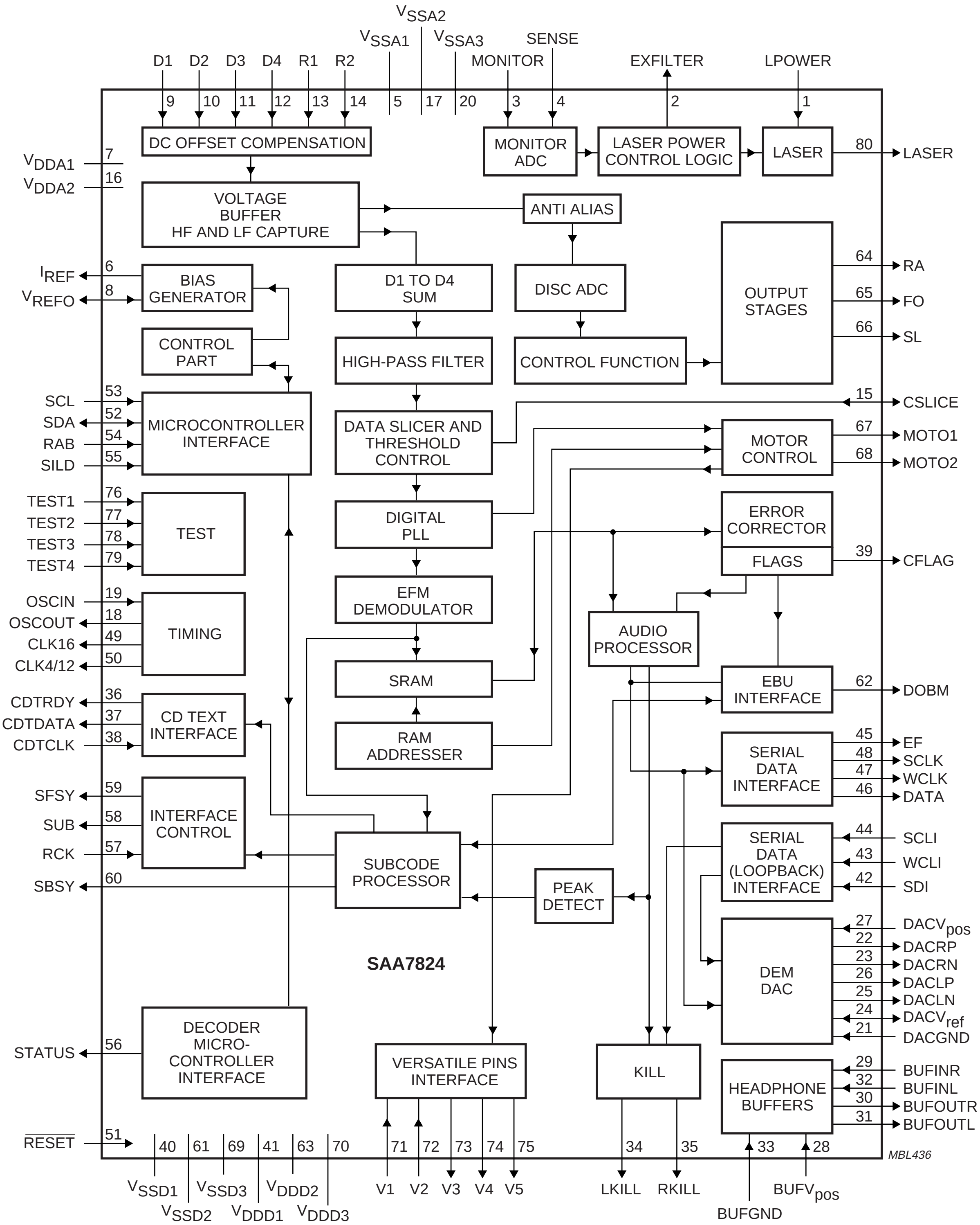



Fig.1 Block diagram.

## 6 PINNING

| SYMBOL | PIN | I/O | DESCRIPTION |
|---|---|---|---|
| LFPOWER | 1 | I | laser power supply |
| EXFILTER | 2 | O | 10 nF capacitor for laser start-up control |
| MONITOR | 3 | I | laser monitor diode |
| SENSE | 4 | I | OPU ground reference point for MONITOR measurement |
| $V_{SSA1}$ | 5 | SUP | analog ground 1 |
| $I_{REF}$ | 6 | O | reference current output (24 kΩ resistor connected to analog ground) |
| $V_{DDA1}$ | 7 | SUP | analog supply voltage 1 |
| $V_{REFO}$ | 8 | I/O | servo reference voltage |
| D1 | 9 | I | diode voltage/current input (central diode signal input) |
| D2 | 10 | I | diode voltage/current input (central diode signal input) |
| D3 | 11 | I | diode voltage/current input (central diode signal input) |
| D4 | 12 | I | diode voltage/current input (central diode signal input) |
| R1 | 13 | I | diode voltage/current input (satellite diode signal input) |
| R2 | 14 | I | diode voltage/current input (satellite diode signal input) |
| CSLICE | 15 | I/O | 10 nF capacitor for adaptive HF data slicer |
| $V_{DDA2}$ | 16 | SUP | analog supply voltage 2 |
| $V_{SSA2}$ | 17 | SUP | analog ground 2 |
| OSCOUT | 18 | O | crystal/resonator output |
| OSCIN | 19 | I | crystal/resonator input |
| $V_{SSA3}$ | 20 | SUP | analog ground 3 |
| DACGND | 21 | I | audio DAC ground |
| DACRP | 22 | O | audio DAC right channel differential positive output |
| DACRN | 23 | O | audio DAC right channel differential negative output |
| $DACV_{ref}$ | 24 | I/O | audio DAC decoupling point (10 µF or 100 nF to ground |
| DACLN | 25 | O | audio DAC left channel differential negative output |
| DACLP | 26 | O | audio DAC left channel differential positive output |
| $DACV_{pos}$ | 27 | I | audio DAC positive supply voltage |
| $BUFV_{pos}$ | 28 | I | audio buffer positive supply voltage |
| BUFINR | 29 | I | audio buffer right input |
| BUFOUTR | 30 | O | audio buffer right output |
| BUFOUTL | 31 | O | audio buffer left output |
| BUFINL | 32 | I | audio buffer left input |
| BUFGND | 33 | I | audio buffer ground |
| LKILL | 34 | O | KILL output for left channel (configurable as open-drain) |
| RKILL | 35 | O | KILL output for right channel (configurable as open-drain) |
| CDTRDY | 36 | O | CD text output to microcontroller ready flag |
| CDTDATA | 37 | O | CD text output data to microcontroller |
| CDTCLK | 38 | I | CD text microcontroller clock input |
| CFLAG | 39 | O | correction flag output (open-drain) |
| $V_{SSD1}$ | 40 | SUP | digital ground 1 |

| SYMBOL | PIN | I/O | DESCRIPTION |
|---|---|---|---|
| $V_{DDD1}$ | 41 | SUP | digital supply voltage 1 |
| SDI | 42 | I | serial data input (loopback) |
| WCLI | 43 | I | word clock input (loopback) |
| SCLI | 44 | I | serial bit clock input (loopback) |
| EF | 45 | O | C2 error flag output |
| DATA | 46 | O | serial data output |
| WCLK | 47 | O | word clock output |
| SCLK | 48 | O | serial clock output |
| CLK16 | 49 | O | 16 MHz clock output |
| CLK4/12 | 50 | O | configurable 4 MHz or 12 MHz clock output |
| $\overline{\text{RESET}}$ | 51 | I | power-on reset input (active LOW) |
| SDA | 52 | I/O | microcontroller interface data input/output (open-drain) |
| SCL | 53 | I | microcontroller interface clock input |
| RAB | 54 | I | microcontroller interface R/W and load control input (4-wire) |
| SILD | 55 | I | microcontroller interface R/W and load control input (4-wire) |
| STATUS | 56 | O | servo interrupt request line/decoder status register/DC offset value readback output |
| RCK | 57 | I | subcode clock input |
| SUB | 58 | O | P to W subcode output |
| SFSY | 59 | O | subcode frame sync output |
| SBSY | 60 | O | subcode block sync output |
| $V_{SSD2}$ | 61 | SUP | digital ground 2 |
| DOBM | 62 | O | bi-phase mark output (externally buffered) |
| $V_{DDD2}$ | 63 | SUP | digital supply voltage 2 |
| RA | 64 | O | radial actuator output |
| FO | 65 | O | focus actuator output |
| SL | 66 | O | sledge actuator output |
| MOTO1 | 67 | O | motor output 1 output |
| MOTO2 | 68 | O | motor output 2 output |
| $V_{SSD3}$ | 69 | SUP | digital ground 3 |
| $V_{DDD3}$ | 70 | SUP | digital supply voltage 3 |
| V1 | 71 | I | versatile pin 1 input |
| V2 | 72 | I | versatile pin 2 input |
| V3 | 73 | O | versatile pin 3 output |
| V4 | 74 | O | versatile pin 4 output |
| V5 | 75 | O | versatile pin 5 output |
| TEST1 | 76 | I | test pin 1 input |
| TEST2 | 77 | I | test pin 2 input |
| TEST3 | 78 | I | test pin 3 input |
| TEST4 | 79 | I | test pin 4 input |
| LASER | 80 | O | laser drive output |

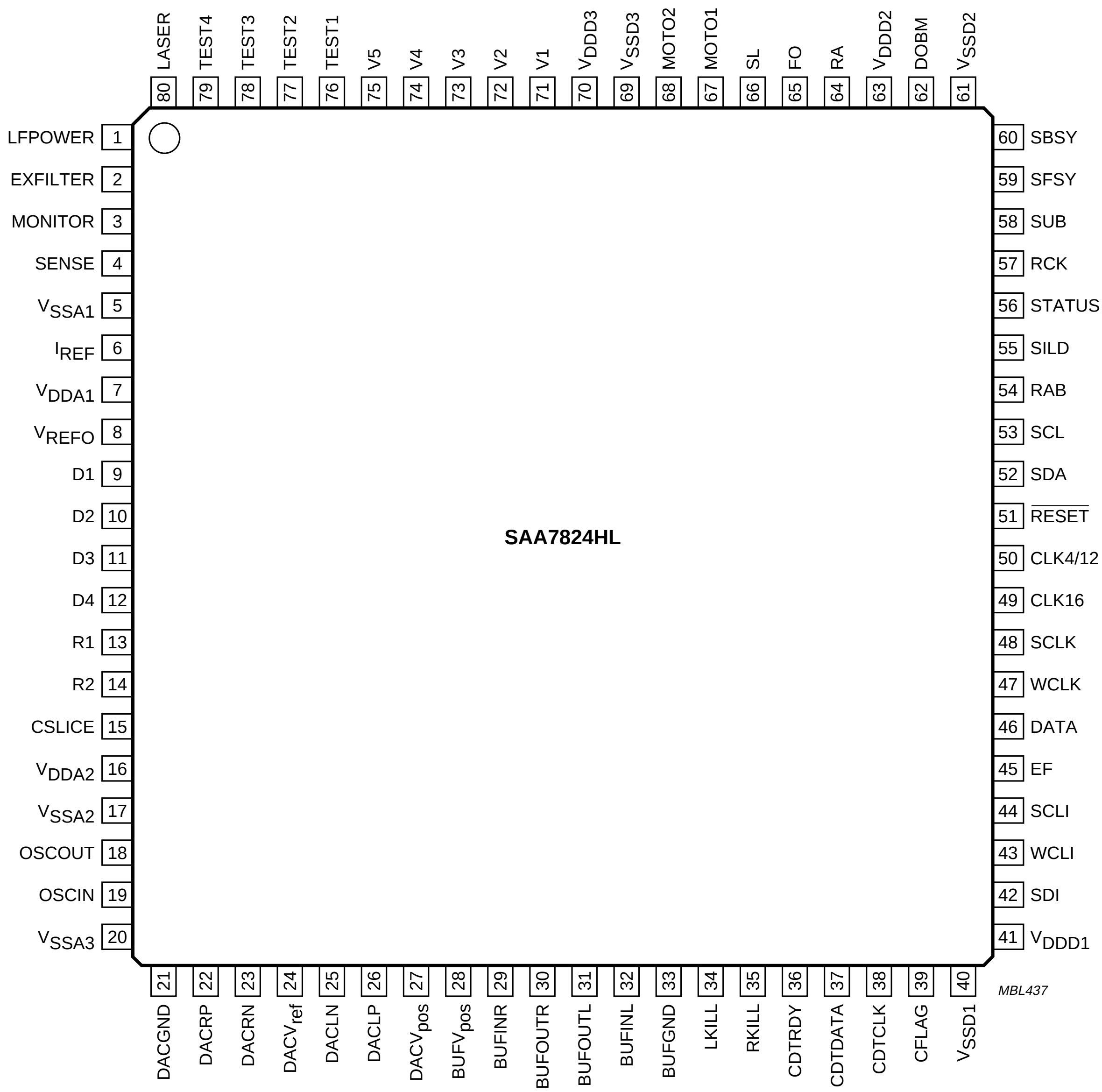



Fig.2 Pin configuration.

## 7 FUNCTIONAL DESCRIPTION

### 7.1 Data acquisition and HF data path

The SAA7824 removes the need for an external diode signal pre-amplifier.

A simplified diagram of the HF data path is illustrated in Fig.3. The high-pass filter, equalizing filter HF gain and adaptive slicer are all register programmable, thus enabling the SAA7824 to be optimized for the intended application.

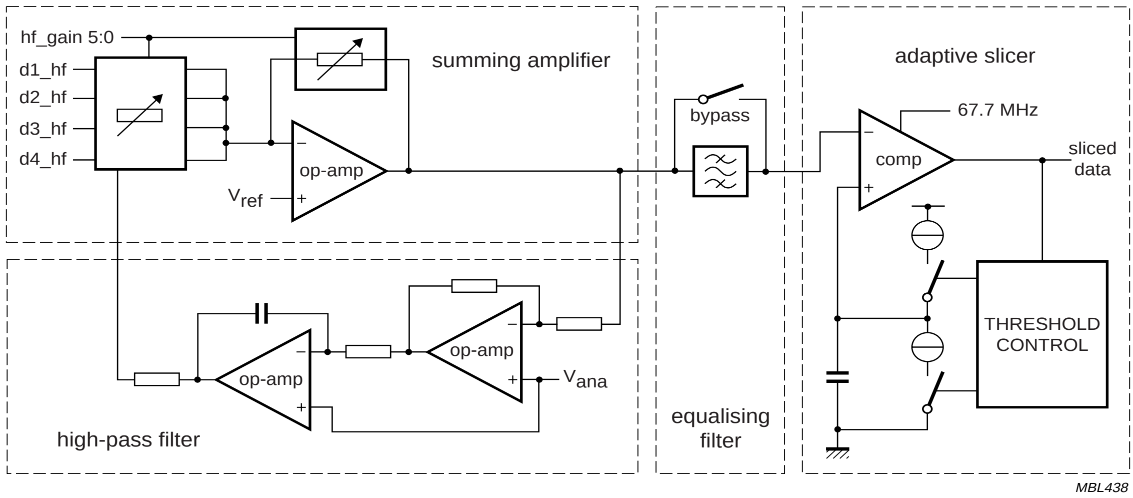



Fig.3 Simplified block diagram of the HF data path and adaptive slicer.

### 7.2 Decoder part

#### 7.2.1 PRINCIPLE OPERATING MODES OF THE DECODER

The decoding part supports a full audio specification and can operate at single-speed (n = 1), double-speed (n = 2) and quad-speed (n = 4). The factor ‘n’ is called the overspeed factor. A simplified data flow through the decoder part is illustrated in Fig.7 for the M0 version and Fig.8 for the M1 version.

#### 7.2.2 DECODER SPEED AND CRYSTAL FREQUENCY

The SAA7824 is a 1×, 2× and 4× (three-speed) decoding device, with an internal Phase-Locked Loop (PLL) clock multiplier. Table 1 gives the playback speeds that are achievable in conjunction with crystal frequency, mechanism, and internal clock settings (selectable via decoder register B).

#### 7.2.3 LOCK-TO-DISC MODE

For electronic shock absorption applications, the SAA7824 can be put into lock-to-disc mode. This allows Constant Angular Velocity (CAV) disc playback with varying input data rates from the inside-to-outside of the disc.

In the lock-to-disc mode, the FIFO is blocked and the decoder will adjust its output data rate to the disc speed. Hence, the frequency of the $I^2S$-bus (WCLK and SCLK) clocks are dependent on the disc speed. In the lock-to-disc mode there is a limit on the maximum variation in disc speed that the SAA7824 will follow. Disc speeds must always be within 25% to 100% range of their nominal value. The lock-to-disc mode is enabled or disabled by decoder register E.

#### 7.2.4 STANDBY MODES

The SAA7824 may be placed in two standby modes, selected by decoder register B (it should be noted that the device core is still active):

- Standby 1: CD STOP mode; most I/O functions are switched off
- Standby 2: CD PAUSE mode; audio output features are switched off, but the motor loop, the motor output and the subcode interfaces remain active; this is also called a ‘Hot Pause’.

In the standby modes the various pins will have the following values:

- MOTO1 and MOTO2: put in to high-impedance, PWM mode (Standby 1 and $\overline{RESET}$: operating in Standby 2); put in high-impedance, PDM mode (Standby 1 and $\overline{RESET}$: operating in Standby 2)
- Pins SCL and SDA: no interaction; normal operation continues
- Pins SCLK, WCLK, DATA, EF and DOBM: 3-state in both standby modes; normal operation continues after reset
- Pins OSCIN, OSCOUT, CLK16 and CLK4/12: no interaction; normal operation continues
- Pins V1 to V5 and CFLAG: no interaction; normal operation continues.

**Table 1** Playback speeds

| REGISTER B | REGISTER E | $f_{xtal}$ = 8.4672 MHz |
|---|---|---|
| 0XXX | 0XXX | n = 1 |
| 1XXX | 0XXX | n = 2; voltage mode only |
| 0XXX | 1XXX | n = 4; voltage mode only |

### 7.3 Crystal oscillator

The crystal oscillator is a conventional 2-pin design which can also operate with ceramic resonators. The external components used around the crystal are illustrated in Fig.4 together with component values (C1 and C2) for a given crystal type given in Table 2. Oscillator frequencies that is used with the SAA7824 is 8.4672 MHz.

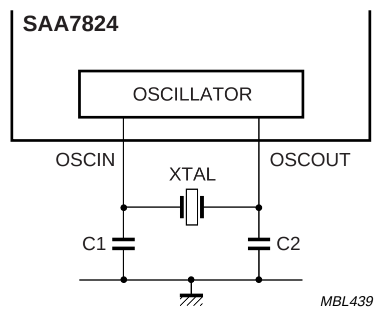



Fig.4 Crystal configuration.

**Table 2** External capacitor selection based upon the crystal type

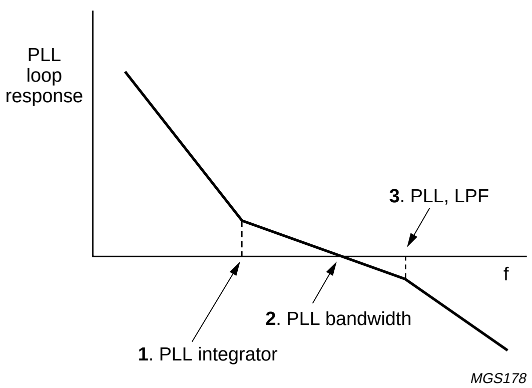
| CRYSTAL LOAD CAPACITANCE ($C_L$) | MAXIMUM SERIES CRYSTAL RESISTANCE ($R_S$) | EXTERNAL LOAD CAPACITORS | |
|---|---|---|---|
| | 8 MHz | C1 | C2 |
| 10 pF | <300 Ω | 8 pF | 8 pF |
| 20 pF | <300 Ω | 27 pF | 27 pF |
| 30 pF | <300 Ω | 47 pF | 47 pF |

### 7.4 Data slicer and bit clock regenerator

The SAA7824 has an integrated adaptive data slicer which is clocked at 67 MHz. The slice level is controlled by internal current sources which are switched onto and integrated by the external capacitor connected to the CSLICE pin. The currents are switched under the control of a Digital Phase-Locked loop (DPLL).

Regeneration of the bit clock is achieved with an internal fully digital PLL. No external components are required and the bit clock is not output. The PLL has two registers (8 and 9) for selecting bandwidth and equalization. The PLL loop response is illustrated in Fig.5.

For certain applications an off-track input is necessary. This is internally connected from the servo part (its polarity can be changed by the foc_parm1 parameter), but may be input via pin V1 if selected by register C. If this flag is HIGH, the SAA7824 will assume that its servo part is following the wrong track, and will flag all incoming HF data as incorrect.




Points 1, 2 and 3 are all programmable via decoder register 8.

Fig.5 Digital PLL loop response.

### 7.5 DC offset cancellation

Unwanted DC offsets can exist within the photo-diode signals and are defined as the DC present in the system when the laser diode is switched off. They arise from various sources of imperfection within the system such as leakage in the photo diodes and offsets in the Optical Pick-Up (OPU) circuitry. The SAA7824 is capable of measuring these offsets and minimizing them.

#### 7.5.1 OFFSET CANCELLATION

A number of registers are associated with the DC offset cancellation function; these registers are given in Table 3.

The measurement time of the DC offset is regulated by new shadow register C (bank 2). A longer time will yield more accurate results but will result in greater measurement durations.

New shadow register 3 (bank 3) is used to select which diode is to be measured.

#### 7.5.2 READING BACK THE DC OFFSET VALUE

The microcontroller needs to be able to read the DC offset measurements in order to calculate the correct cancellation value [for writing back to new shadow register 7 (bank 3)].

This is achieved by using the STATUS pin and setting decoder register 7 to XX10. Shadow register C (bank 3) can then be used to control the STATUS pin output; the register settings are given in Table 20.

Once the measurement time has been set and the diode selected, the STATUS pin should be set to read the DC offset ready flag [new shadow register C (bank 3) = X01X]. This signal will toggle HIGH after the prescribed measurement time. Changing the diode selection will result in the measurement timer being automatically reset.

The microcontroller can read back the measurement by setting the STATUS pin to output the DC offset value [new shadow register C (bank 3) = X10X].

The offset value is repeatedly streamed out through the STATUS pin and is UART compatible. It should be noted that the MSB is inverted and will require re-inverting after the offset value has been captured. Timing information for this signal is illustrated in Fig.6.

The final DC cancellation value (as calculated by the microcontroller) can then be written to new shadow register 7 (bank 3). This is a multiple write register containing the cancellation values for all six diodes.

**Table 3** Registers relating to the DC offset cancellation

| SHADEN BITS | SHADOW REGISTER | ADDRESS | DATA | FUNCTION | INITIAL |
|---|---|---|---|---|---|
| 10 (bank 2) | C DC offset measurement times | 1100 | XX00 | settling time = 354 μs | reset |
| | | | XX01 | settling time = 1 ms | – |
| | | | XX10 | settling time = 2 ms | – |
| | | | XX11 | settling time = 10 ms | – |
| 11 (bank 3) | 3 diode selection for DC offset measurement | 0011 | 0000 | select D1 | reset |
| | | | 0001 | select D1 | – |
| | | | 0010 | select D2 | – |
| | | | 0011 | select D3 | – |
| | | | 0100 | select D4 | – |
| | | | 0101 | select R1 | – |
| | | | 0110 | select R2 | – |
| | | | 0111 | select D1 | – |
| | C STATUS pin control | 1100 | X00X | STATUS pin outputs decoder status register information | reset |
| | | | X01X | STATUS pin outputs DC offset ready flag | – |
| | | | X10X | STATUS pin outputs DC offset value | – |
| | 7 DC cancellation levels | 0111 | multi-write (9 × 4 bits) | DC cancellation values for diodes D1 to D4 and R1 and R2; see Table 20 | – |

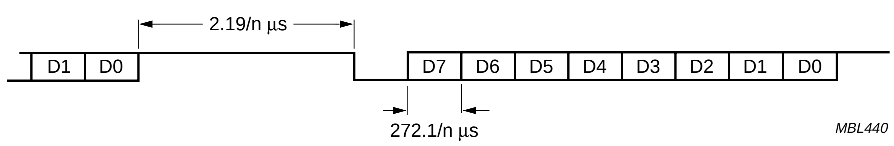



Fig.6 Serial data format for DC offset data.

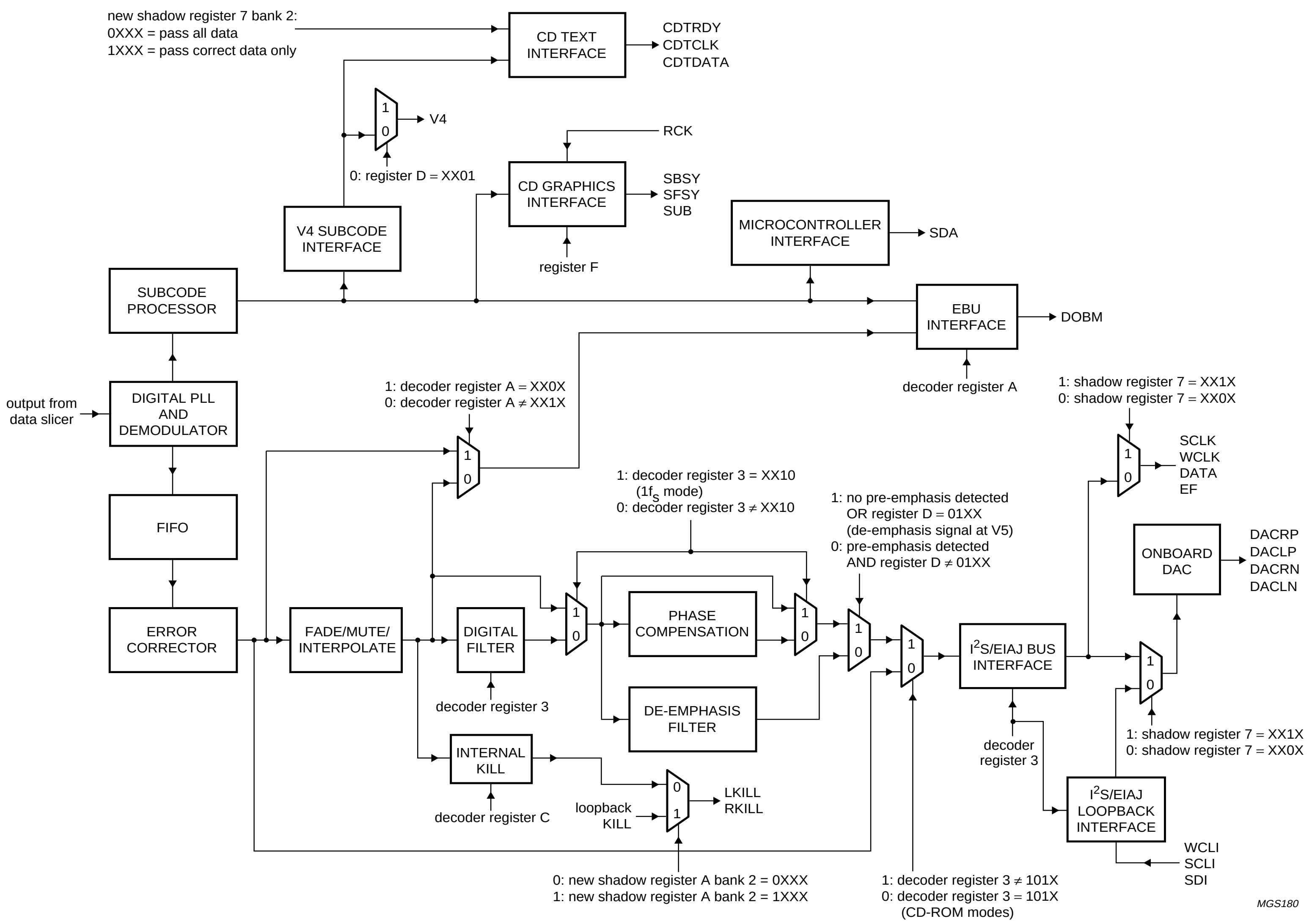



Fig.7 Simplified data flow of decoder functions for the M0 version.

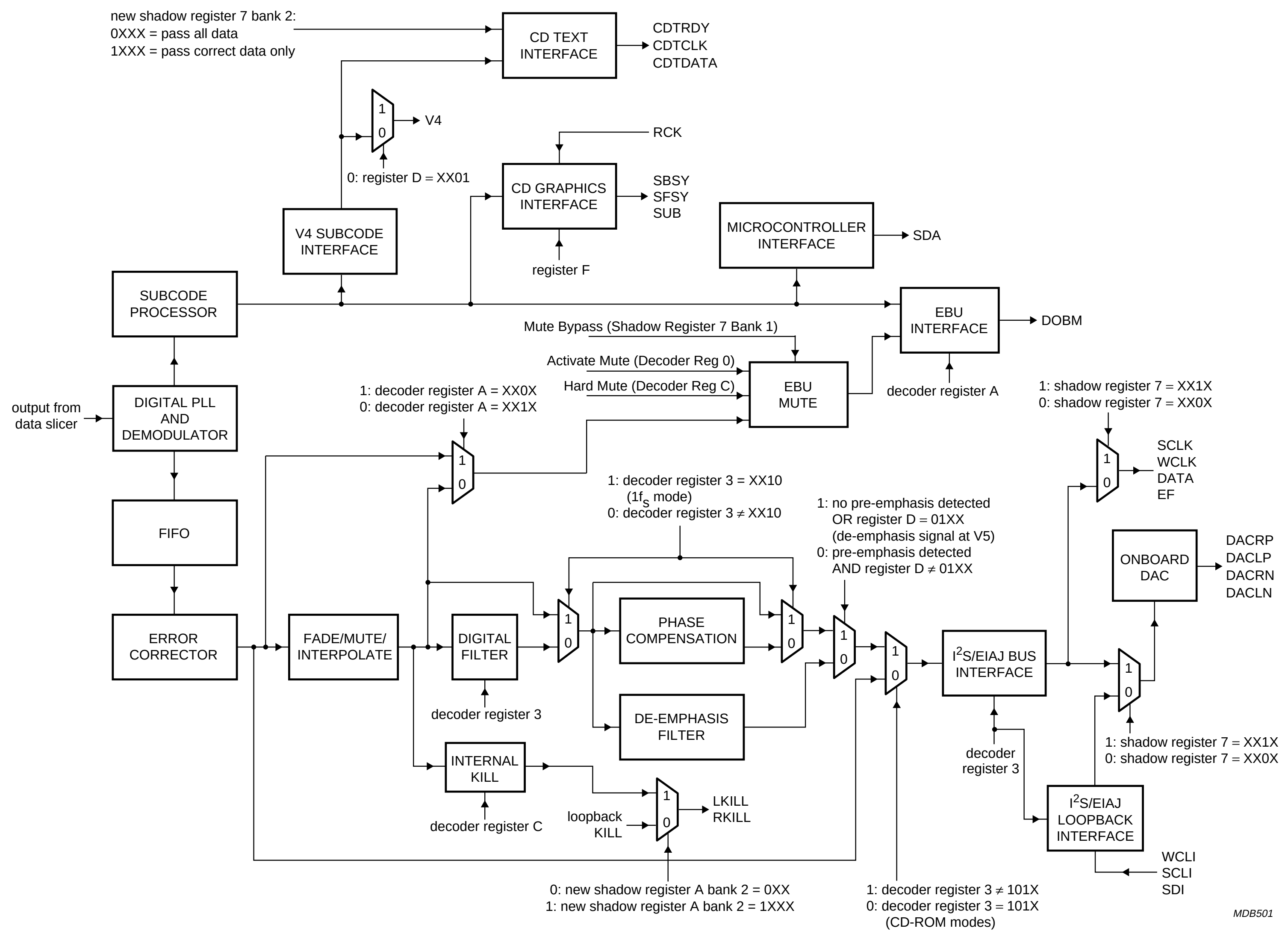



Fig.8 Simplified data flow of decoder functions for the M1 version.

### 7.6 Demodulator

#### 7.6.1 FRAME SYNC PROTECTION

A double timing system is used to protect the demodulator from erroneous sync patterns in the serial data. The master counter is only reset if:

- A sync coincidence is detected; sync pattern occurs 588 ±1 EFM clocks after the previous sync pattern
- A new sync pattern is detected within ±6 EFM clocks of its expected position.

The sync coincidence signal is also used to generate the PLL lock signal, which is active HIGH after 1 sync coincidence is found, and reset LOW if during 61 consecutive frames no sync coincidence is found. The PLL lock signal can be accessed via the SDA or STATUS pins selected by decoder registers 2, 7 and new shadow register C (bank 3).

Also incorporated in the demodulator is a Run Length 2 (RL2) correction circuit. Every symbol detected as RL2 will be pushed back to RL3. To do this, the phase error of both edges of the RL2 symbol are compared and the correction is executed at the side with the highest error probability.

#### 7.6.2 EFM DEMODULATION

The 14-bit EFM data and subcode words are decoded into 8-bit symbols.

### 7.7 Subcode data processing

#### 7.7.1 Q-CHANNEL PROCESSING

The 96-bit Q-channel word is accumulated in an internal buffer. The last 16 bits are used internally to perform a Cyclic Redundancy Check (CRC). If the data is good, the SUBQREADY-I signal will go LOW. SUBQREADY-I can be read via the SDA or STATUS pins, selected via decoder registers 2, 7 and new shadow register C (bank 3). Good Q-channel data may be read from pin SDA.

#### 7.7.2 EIAJ 3 AND 4-WIRE SUBCODE (CD GRAPHICS) INTERFACE

Data from all the subcode channels (P-to-W) may be read via the subcode interface, which conforms to EIAJ CP-2401. The interface is enabled and configured as either a 3 or 4-wire interface via decoder register F.

The subcode interface output formats are illustrated in Fig.9, where the RCK signal is supplied by another device such as a CD graphics decoder.

#### 7.7.3 V4 SUBCODE INTERFACE

Data of subcode channels, Q-to-W, may be read via pin V4 if selected via decoder register D. The format is similar to RS232 and is illustrated in Fig.10. The subcode sync word is formed by a pause of (200/n) µs minimum. Each subcode byte starts with a logic 1 followed by 7 bits (Q-to-W). The gap between bytes is variable between (11.3/n) µs and (90/n) µs.

The subcode data is also available in the EBU output (DOBM) in a similar format.

#### 7.7.4 CD TEXT INTERFACE

R-to-W subcode data is captured and stored until a complete CD text PACK is formed. The least significant 16 bits of the PACK are used for a CRC.

The behaviour of the CD text interface is controlled by new shadow register 7 (bank 2). The interface can either flag all data (i.e. passed or failed CRC) or it can flag good data only.

The data ready flag is monitored via pin CDTRDY and is active LOW. The pulse width varies from 73/n µs, for the first three packs, to 317/n µs for the fourth pack.

When a PACK becomes available, the initial value of the CDTDATA pin indicates the CRC result (HIGH = passed; LOW = failed). The microcontroller can fetch the data by applying a clock signal (maximum frequency = 5 MHz) to pin CDTCLK and reading the subsequent bitstream on pin CDTDATA.

The 128 data bits are streamed out LSB first. A complete CD text PACK consists of 4 header bytes, 12 data bytes, and 2 CRC bytes although the latter 2 bytes are dropped internally once the CRC calculation is complete. Please refer to the *“Red Book”* for further details relating to the format of a CD text PACK

The timing diagram for the CD text interface is illustrated in Fig.11.

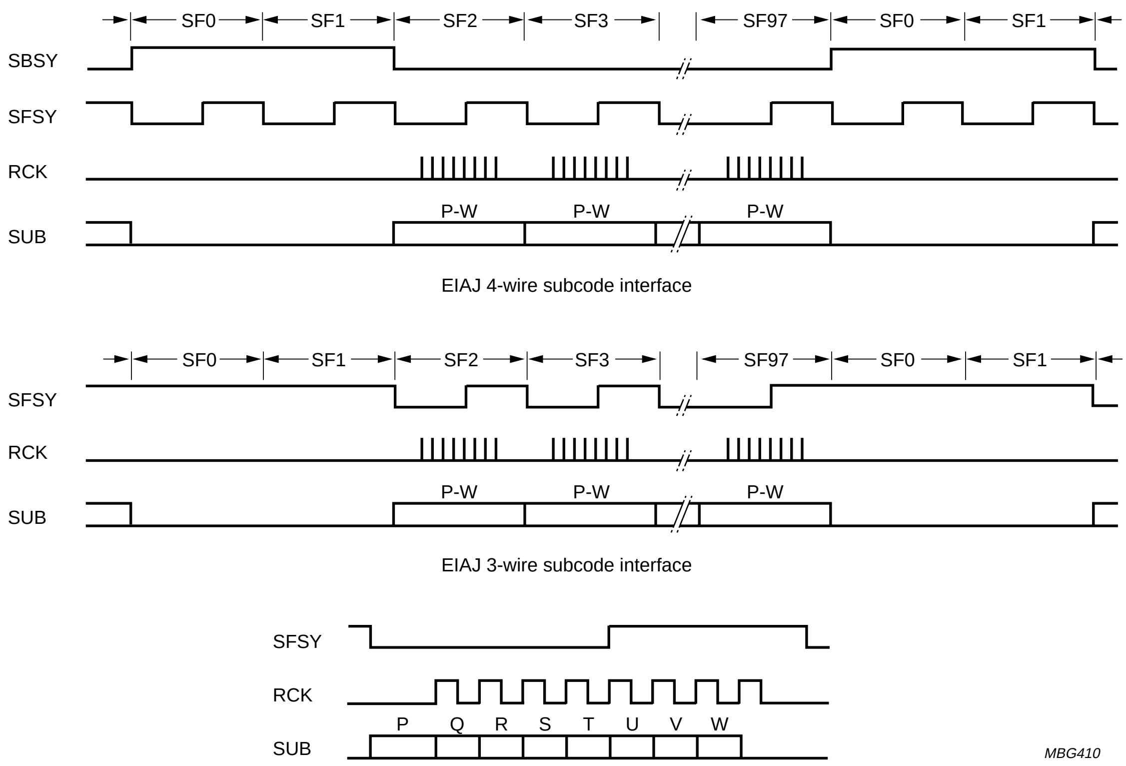
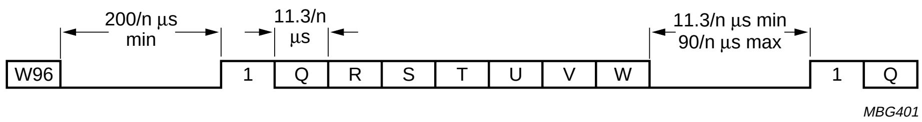
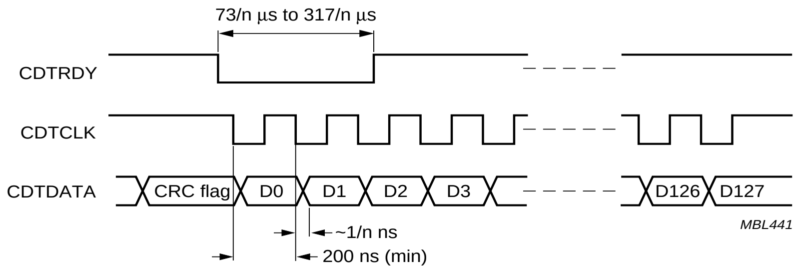



Fig.9 EIAJ subcode (CD graphics) interface format.




Where n = disc speed.

Fig.10 Subcode format and timing on pin V4.




Where n = disc speed.

Fig.11 CD text interface format and timing.

### 7.8 FIFO and error correction

The SAA7824 has a ±8 frame FIFO. The error corrector is a t = 2, e = 4 type, with error corrections on both C1 (32 symbol) and C2 (28 symbol) frames. Four symbols are used from each frame as parity symbols. This error corrector can correct up to two errors on the C1 level and up to four errors on the C2 level.

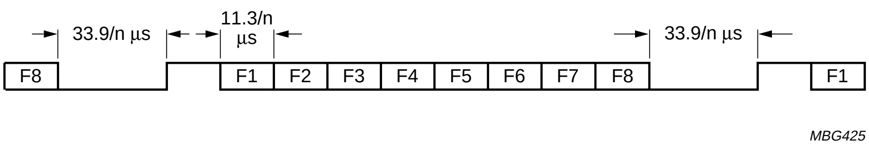
The error corrector also contains a flag processor. Flags are assigned to symbols when the error corrector cannot ascertain if the symbols are definitely good. C1 generates output flags which are read after de-interleaving by C2, to help in the generation of C2 output flags.

The C2 output flags are used by the interpolator for concealment of uncorrectable errors. They are also output via the EBU signal (DOBM). The EF output will flag bytes in error in both audio and CD-ROM modes.

#### 7.8.1 FLAGS OUTPUT (CFLG)

The flags output pin CFLG shows the status of the error corrector and interpolator and is updated every frame (7.35 × n kHz). In the SAA7824, 8 × 1-bit flags are present on the CFLG pin as illustrated in Fig.12. This signal shows the status of the error corrector and interpolator.

The first flag bit, F1, is the absolute time sync signal, the FIFO-passed subcode sync and relates the position of the subcode sync to the audio data (DAC output). This flag may also be used in a super FIFO or in the synchronization of different players. The output flags can be made available at bit 4 of the EBU data format (LSB of the 24-bit data word), if selected by decoder register A.




Where n = disc speed.

Fig.12 Flag output timing diagram.

**Table 4** Output flags

| F1 | F2 | F3 | F4 | F5 | F6 | F7 | F8 | DESCRIPTION |
|---|---|---|---|---|---|---|---|---|
| 0 | X | X | X | X | X | X | X | no absolute time sync |
| 1 | X | X | X | X | X | X | X | absolute time sync |
| X | 0 | 0 | X | X | X | X | X | C1 frame contained no errors |
| X | 0 | 1 | X | X | X | X | X | C1 frame contained 1 error |
| X | 1 | 0 | X | X | X | X | X | C1 frame contained 2 errors |
| X | 1 | 1 | X | X | X | X | X | C1 frame uncorrectable |
| X | X | X | 0 | 0 | X | X | 0 | C2 frame contained no errors |
| X | X | X | 0 | 0 | X | X | 1 | C2 frame contained 1 error |
| X | X | X | 0 | 1 | X | X | 0 | C2 frame contained 2 errors |
| X | X | X | 0 | 1 | X | X | 1 | C2 frame contained 3 errors |
| X | X | X | 1 | 0 | X | X | 0 | C2 frame contained 4 errors |
| X | X | X | 1 | 1 | X | X | 1 | C2 frame uncorrectable |
| X | X | X | X | X | 0 | 0 | X | no interpolations |
| X | X | X | X | X | 0 | 1 | X | at least one 1-sample interpolation |
| X | X | X | X | X | 1 | 0 | X | at least one hold and no interpolations |
| X | X | X | X | X | 1 | 1 | X | at least one hold and one 1-sample interpolation |

### 7.9 Audio functions

#### 7.9.1 DE-EMPHASIS AND PHASE LINEARITY

When pre-emphasis is detected in the Q-channel subcode, the digital filter automatically includes a de-emphasis filter section. When de-emphasis is not required, a phase compensation filter section controls the phase of the digital oversampling filter to ≤ ±1° within the band 0 to 16 kHz. With de-emphasis the filter is not phase linear.

If the de-emphasis signal is set to be available at pin V5, selected via decoder register D, then the de-emphasis filter is bypassed.

#### 7.9.2 DIGITAL OVERSAMPLING FILTER

For optimizing performance with an external DAC, the SAA7824 contains a 2 to 4 times oversampling IIR filter. The filter specification of the 4 times oversampling filter is given in Table 5.

These attenuations do not include the sample-and-hold at the external DAC output or the DAC post filter. When using the oversampling filter, the output level is scaled –0.5 dB down to avoid overflow on full-scale sine wave inputs (0 to 20 kHz).

**Table 5** Filter specification

| PASS BAND | STOP BAND | ATTENUATION |
|---|---|---|
| 0 to 9 kHz | – | ≤0.001 dB |
| 19 to 20 kHz | – | ≤0.03 dB |
| – | 24 kHz | ≥25 dB |
| – | 24 to 27 kHz | ≥38 dB |
| – | 27 to 35 kHz | ≥40 dB |
| – | 35 to 64 kHz | ≥50 dB |
| – | 64 to 68 kHz | ≥31 dB |
| – | 68 kHz | ≥35 dB |
| – | 69 to 88 kHz | ≥40 dB |

#### 7.9.3 CONCEALMENT

A 1-sample linear interpolator becomes active if a single sample is flagged as erroneous but cannot be corrected. The erroneous sample is replaced by a level midway between the preceding and following samples. Left and right channels have independent interpolators. If more than one consecutive non-correctable sample is found, the last good sample is held. A 1-sample linear interpolation is then performed before the next good sample; see Fig.13.

In CD-ROM modes (i.e. the external DAC interface is selected to be in a CD-ROM format) concealment is not executed.

#### 7.9.4 MUTE, FULL-SCALE, ATTENUATION AND FADE

A digital level controller is present on the SAA7824 which performs the functions of soft mute, full-scale, attenuation and fade; these are selected via decoder register 0:

- Mute: signal reduced to 0 in a maximum of 128 steps; 3/n ms
- Attenuation: signal scaled by –12 dB
- Full-scale: ramp signal back to 0 dB level; from mute it takes 3/n ms
- Fade: activates a 128 stage counter which allows the signal to be scaled up or down in 0.07 dB steps
  - 128 = full-scale
  - 120 = –0.5 dB (i.e. full-scale if oversampling filter is used)
  - 32 = –12 dB
  - 0 = mute.

#### 7.9.5 PEAK DETECTOR

The peak detector measures the highest audio level (absolute value) on positive peaks for left and right channels. The 8 most significant bits are output in the Q-channel data in place of the CRC bits. Bits 81 to 88 contain the left peak value (bit 88 = MSB) and bits 89 to 96 contain the right peak value (bit 96 = MSB). The values are reset after reading Q-channel data via pin SDA.

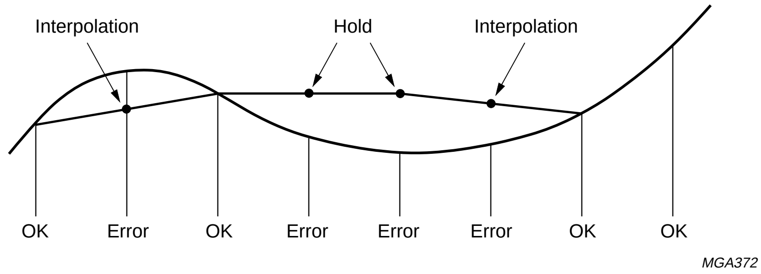



Fig.13 Concealment mechanism.

### 7.10 Audio DAC interface

#### 7.10.1 INTERNAL DYNAMIC ELEMENT MATCHING DIGITAL-TO-ANALOG CONVERTER

The onboard audio DEM DAC operates at an oversampling rate of $96f_s$ and is designed for operation with an audio input at $1f_s$. The DAC is equipped with two pairs of stereo outputs for driving medium impedance line outputs and for directly driving low impedance headphones. A pair of analog inputs are provided to enable external audio sources to make use of the headphone output buffers.

Audio data from the decoder part of the SAA7824 can be routed as described in Sections 7.10.1.1 and 7.10.1.2.

**Table 6** Shadow register

| SHADEN BITS | SHADOW REGISTER | ADDRESS | DATA | FUNCTION | RESET |
|---|---|---|---|---|---|
| 01 (bank 1) | 7 control of onboard DAC | 0111 | 0000 | use external DAC or route audio data back into onboard DAC (loopback mode) | reset |
| | | | 0010 | route audio data directly into onboard DAC (non-loopback mode) | – |

##### *7.10.1.1 Use of internal DAC*

Setting shadow register 7 to 0010 will route audio data from the decoder into the internal DAC. To enable the on-board DAC, the DAC interface format (set by register 3) must be set to 16-bit $1f_s$ mode, either $I^2S$-bus or EIAJ format. CD-ROM mode can also be used if interpolation is not required. The serial data output pins for interfacing with an external DAC (SCLK, WCLK, DATA and EF) are set to high-impedance.

*7.10.1.2 Loopback external data into onboard DAC*

The onboard DAC can also be set to accept serial data inputs from an external source, e.g. an Electronic Shock Absorption (ESA) IC. This is known as loopback mode and is enabled by setting shadow register 7 to 0000. This enables the serial data output pins (SCLK, WCLK, DATA and EF) so that data can be routed from the SAA7824 to an external ESA system (or external DAC).

The serial data from an external ESA IC can then also be input to the onboard DAC on the SAA7824 by utilising the serial data input interface (SCLI, SDI and WCLI).

In this mode, a wide range of data formats to the external ESA IC can be programmed as shown in Table 7. However, the serial input on the SAA7824 will always expect the input data from the ESA IC to be 16-bit $1f_s$ and the same data format, either $I^2S$-bus or EIAJ, as the serial output format (set by decoder register 3).

7.10.2 EXTERNAL DAC INTERFACE

Audio data from the SAA7824 can be sent to an external DAC, identical to the SAA732x series, in 'loopback' mode (i.e. shadow register 7 is set to 0000).

The SAA7824 is compatible with a wide range of external DACs. Eleven formats are supported and are given in Table 7. Figures 14 and 15 show the Philips $I^2S$-bus and the EIAJ data formats respectively. When the decoder is operated in lock-to-disc mode, the SCLK frequency is dependent on the disc speed factor 'd'.

All formats are MSB first and $1f_s$ is 44.1 kHz. The polarity of the WCLK and the data can be inverted; selectable by decoder register 7. It should be noted that EF is only a defined output in CD-ROM and $1f_s$ modes.

When using an external DAC (or when using the onboard DAC in non-loopback mode), the serial data inputs to the onboard DAC (SCLI, SDI and WCLI) should be tied to ground.

**Table 7** DAC interface formats

| REGISTER 3 | SAMPLE FREQUENCY | NUMBER OF BITS | SCLK (MHz) | FORMAT | INTERPOLATION |
|---|---|---|---|---|---|
| 1010 | $f_s$ | 16 | $2.1168 \times n$ | CD-ROM ($I^2S$-bus) | no |
| 1011 | $f_s$ | 16 | $2.1168 \times n$ | CD-ROM (EIAJ) | no |
| 1110 | $f_s$ | 16/18(1) | $2.1168 \times n$ | Philips $I^2S$-bus 16/18 bits(1) | yes |
| 0010 | $f_s$ | 16 | $2.1168 \times n$ | EIAJ 16 bits | yes |
| 0110 | $f_s$ | 18 | $2.1168 \times n$ | EIAJ 18 bits | yes |
| 0000 | $4f_s$ | 16 | $8.4672 \times n$ | EIAJ 16 bits | yes |
| 0100 | $4f_s$ | 18 | $8.4672 \times n$ | EIAJ 18 bits | yes |
| 1100 | $4f_s$ | 18 | $8.4672 \times n$ | Philips $I^2S$-bus 18 bits | yes |
| 0011 | $2f_s$ | 16 | $4.2336 \times n$ | EIAJ 16 bits | yes |
| 0111 | $2f_s$ | 18 | $4.2336 \times n$ | EIAJ 18 bits | yes |
| 1111 | $2f_s$ | 18 | $4.2336 \times n$ | Philips $I^2S$-bus 18 bits | yes |

**Note**

1. In this mode the first 16 bits contain data, but if any of the fade, attenuate or de-emphasis filter functions are activated then the first 18 bits contain data.

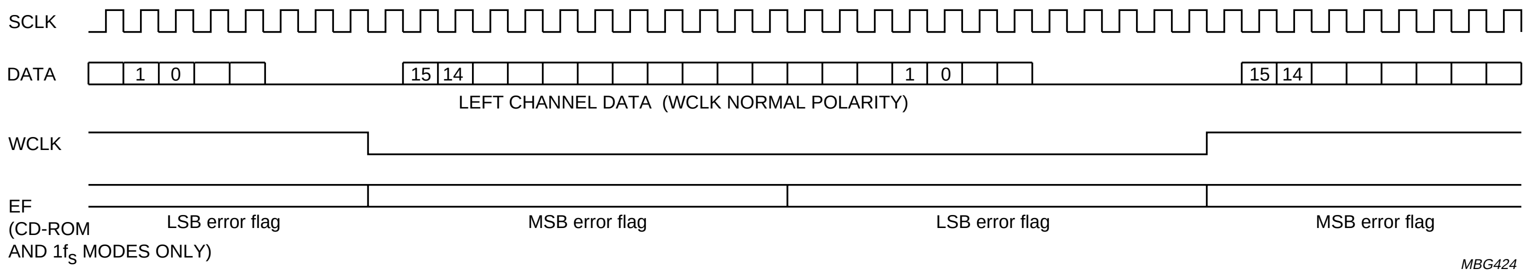



Fig.14 Philips I$^2$S-bus data format (16-bit word length).

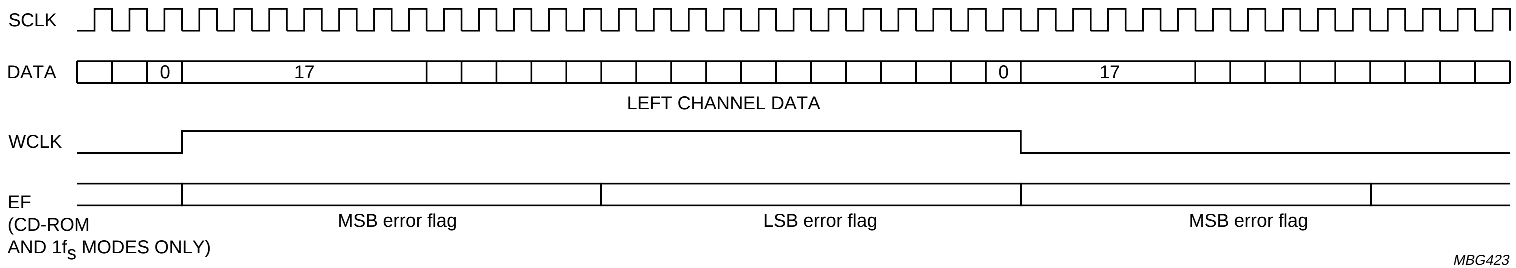



Fig.15 EIAJ data format (18-bit word length).

### 7.11 EBU interface

The bi-phase mark digital output signal at pin DOBM is in accordance with the format defined by the IEC 60958 specification. Three different modes can be selected via decoder register A:

- DOBM pin held LOW
- Data taken before concealment, mute and fade (must always be used for CD-ROM modes)
- Data taken after concealment, mute and fade.

An additional mute function is available via shadow register 7 (bank 1) and decoder register 0 and C. They provide the following:

- Hard mute: immediate mute of the audio sample in the ROM mode at 1×, 2× or 4×
- Soft mute: 3 ms ramp up or ramp down of the audio samples in the 1× audio mode
- Bypass: switches the EBU mute function out of the EBU signal path.

#### 7.11.1 FORMAT

The digital audio output consists of 32-bit words (‘subframes’) transmitted in bi-phase mark code (two transitions for a logic 1 and one transition for a logic 0). Words are transmitted in blocks of 384. The EBU frame format is given in Table 8.

**Table 8** EBU frame format; see also Table 9

| FUNCTION | BITS | DESCRIPTION |
|---|---|---|
| Sync | 0 to 3 | – |
| Auxiliary | 4 to 7 | not used; normally zero |
| Error flags | 4 | CFLG error and interpolation flags when selected by register A |
| Audio sample | 8 to 27 | first 4 bits not used (always zero); twos complement; LSB = bit 12, MSB = bit 27 |
| Validity flag | 28 | valid = logic 0 |
| User data | 29 | used for subcode data (Q-to-W) |
| Channel status | 30 | control bits and category code |

**Table 9** Description of EBU frame function

| FUNCTION | DESCRIPTION |
|---|---|
| Sync | The sync word is formed by violation of the bi-phase rule and therefore does not contain any data. Its length is equivalent to 4 data bits. The 3 different sync patterns indicate the following situations: sync B; start of a block (384 words), word contains left sample; sync M; word contains left sample (no block start) and sync W; word contains right sample. |
| Audio sample | Left and right samples are transmitted alternately. |
| Validity flag | Audio samples are flagged (bit 28 = 1) if an error has been detected but was uncorrectable. This flag remains the same even if data is taken after concealment. |
| User data | Subcode bits Q-to-W from the subcode section are transmitted via the user data bit. This data is asynchronous with the block rate. |
| Channel status | The channel status bit is the same for left and right words. Therefore a block of 384 words contains 192 channel status bits. The category code is always CD. The bit assignment is given in Table 10. |

**Table 10** Bit assignment

| FUNCTION | BITS | DESCRIPTION |
|---|---|---|
| Control | 0 to 3 | copy of CRC checked Q-channel control bits 0 to 3; bit 2 is logic 1 when copy permitted; bit 3 is logic 1 when recording has pre-emphasis |
| Reserved mode | 4 to 7 | always zero |
| Category code | 8 to 15 | CD: bit 8 = logic 1, all other bits = logic 0 |
| Clock accuracy | 28 to 29 | set by register A; 10 = level I; 00 = level II; 01 = level III |
| Remaining | 6 to 27 and 30 to 191 | always zero |

## 7.12 KILL features

### 7.12.1 THE KILL CIRCUIT

The KILL circuit detects digital silence by testing for an all-zero or all-ones data word in the left and right channels. This occurs in two places; prior to the digital filter (internal KILL), and in the digital DAC (loopback/external KILL). Programming bit 3 of new shadow register A (bank 2) determines whether internal or external data is used. The output is switched to active HIGH when silence has been detected for at least 270 ms, or if mute is active, or in CD-ROM mode. Two KILL modes are available which can be selected by decoder register C:

- Mono KILL: LKILL and RKILL are both active HIGH when silence is detected on left and right channels simultaneously
- Stereo KILL: LKILL and RKILL are active HIGH independently of each other when silence is detected on either channel.

### 7.12.2 SILENCE INJECTION

The silence inject function monitors the left and right KILL signals and forces the analog DAC into silence when KILL is asserted. This improves the internal Signal-to-Noise Ratio (SNR) by preventing any spurious noise from reaching the DAC. The silence inject function can be enabled or disabled by programming bit 2 of the new shadow register A (bank 2).

## 7.13 Audio features off

The audio features can be turned off (selected by decoder register E) and will affect the following functions:

- Digital filter, fade, peak detector, internal KILL circuit (although RKILL and LKILL outputs still active) are disabled
- V5 (if selected to be the de-emphasis flag output) and the EBU outputs become undefined.

The EBU output should be set LOW prior to switching the audio features off and after switching the audio features back on, a full-scale command should be given.

## 7.14 The versatile pins interface

The SAA7824 has five pins that can be reconfigured for different applications.

The functions of these versatile pins are identical to the SAA732x series and can be programmed by decoder registers C, D and shadow register 3 (bank 1) as shown in Table 11.

**Table 11** Pin applications

| PIN NAME | PIN NUMBER | TYPE | REGISTER ADDRESS | REGISTER DATA | FUNCTION |
|---|---|---|---|---|---|
| V1 | 71 | input | 1100 | XXX1 | external off-track signal input |
| | | | – | XXX0 | internal off-track signal used input may be read via decoder status bit; selected via register 2 |
| V2 | 72 | input | – | – | input may be read via decoder status bit; selected via register 2 |
| V3 | 73 | output | 1100 | 00XX | output = 0 |
| | | | – | 01XX | output = 1 |
| V4 | 74 | output | 1101 | 0000 | 4-line motor drive (using V4 and V5) |
| | | | – | XX01 | Q-to-W subcode output |
| | | | – | XX10 | output = 0 |
| | | | – | XX11 | output = 1 |
| V5 | 75 | output | 1101 | 01XX | de-emphasis output (active HIGH) |
| | | | – | 10XX | output = 0 |
| | | | – | 11XX | output = 1 |

### 7.15 Spindle motor control

#### 7.15.1 MOTOR OUTPUT MODES

The spindle motor speed is controlled by a fully integrated digital servo. Address information from the internal ±8 frame FIFO and disc speed information are used to calculate the motor control output signals. Several output modes, selected by decoder register 6, are supported:

- Pulse density, 2-line (true complement output), $(1 \times n)$ MHz sample frequency
- PWM output, 2-line, $(22.05 \times n)$ kHz modulation frequency
- PWM output, 4-line, $(22.05 \times n)$ kHz modulation frequency
- CDV motor mode.

##### *7.15.1.1 Pulse density output mode*

In the pulse density mode the motor output pin (MOTO1) is the pulse density modulated motor output signal.

A 50% duty factor corresponds with the motor not actuated, higher duty factors mean acceleration, lower duty factors means braking. In this mode, the MOTO2 signal is the inverse of the MOTO1 signal. Both signals change state only on the edges of a $(1 \times n)$ MHz internal clock signal.

##### *7.15.1.2 PWM output mode (2-line)*

In the PWM mode the motor acceleration signal is put in pulse-width modulation form on the MOTO1 output. The motor braking signal is pulse-width modulated on the MOTO2 output. The timing is illustrated in Fig 16. A typical application diagram is illustrated in Fig 17.

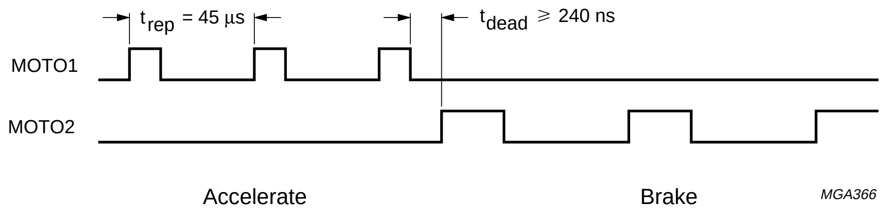



Fig.16 2-line PWM mode timing.

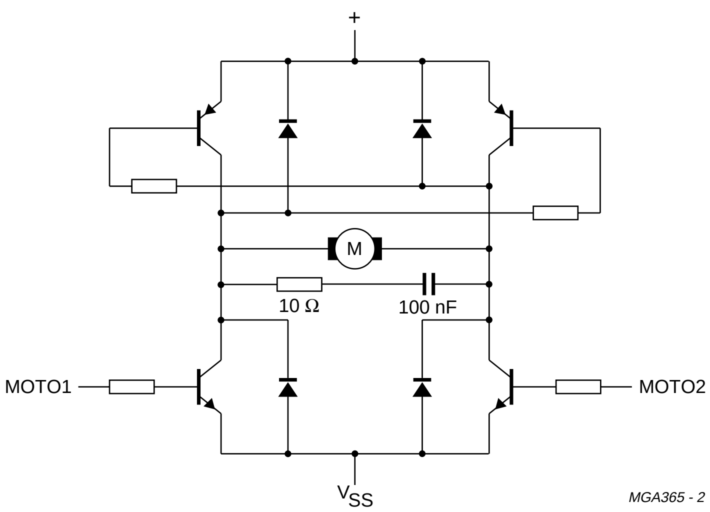



Fig.17 Motor 2-line PWM mode application diagram.

*7.15.1.3 PWM output mode (4-line)*

Using two extra outputs from the versatile pins interface, it is possible to use the SAA7824 with a 4-input motor bridge. The timing is illustrated in Fig 18. A typical application diagram is illustrated in Fig 19.

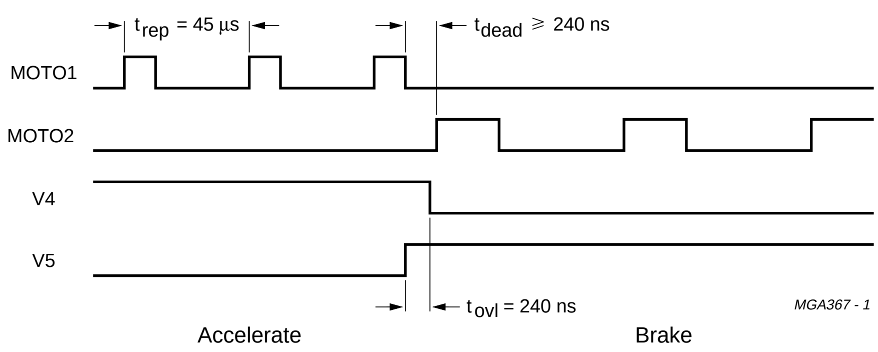



Fig.18 4-line PWM mode timing.

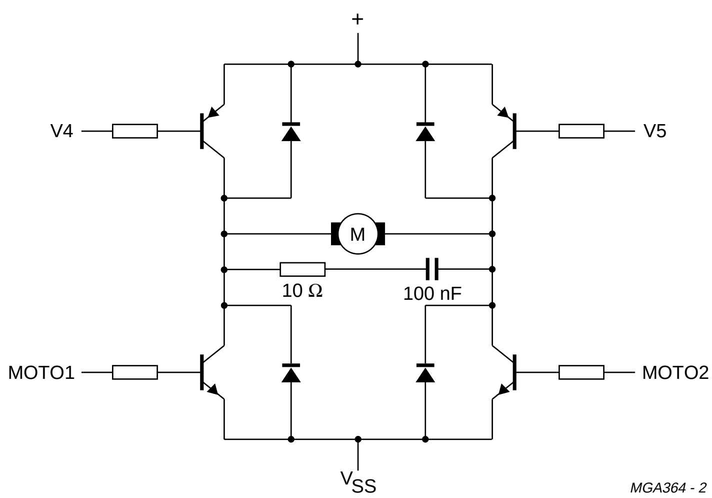



Fig.19 Motor 4-line PWM mode application diagram.

#### *7.15.1.4 CDV/CAV output mode*

In the CDV motor mode, the FIFO position will be put in pulse-width modulated form on the MOTO1 pin [carrier frequency (300 × d) Hz], where 'd' is the disc speed factor. The PLL frequency signal will be put in pulse-density modulated form (carrier frequency 4.23 × n MHz) on the MOTO2 pin. The integrated motor servo is disabled in this mode.

The PWM signal on MOTO1 corresponds to a total memory space of 20 frames, therefore the nominal FIFO position (half full) will result in a PWM output of 60%.

In the lock-to-disc (CAV) mode the CDV motor mode is the only mode that can be used to control the motor.

### 7.15.2 SPINDLE MOTOR OPERATING MODES

The operating modes of the motor servo are controlled by decoder register 1; see Table 12.

In the SAA7824 decoder there is an anti-windup mode for the motor servo, selected via decoder register 1. When the anti-windup mode is activated the motor servo integrator will hold if the motor output saturates.

#### *7.15.2.1 Motor OV flag*

The SAA7824 contains a servo loop that is used to regulate the spindle speed. The motor OV flag is provided to indicate when the motor output has overloaded. During a large change in disc speed i.e. by a long jump or x-factor change, the motor OV flag will be asserted due to the full and longer duration required to attain the new desired speed.

The OV flag indicates when the internal processes of the modulator have overflowed and not necessarily when the output power has reached 100%. Similarly, the flag does not fall at a specific output power level but at a specific speed error level. The error level at which the flag falls is determined by the selected servo gain, and will be internally equivalent to +3 × gain or –3 × gain.

#### *7.15.2.2 Power limit*

In start mode 1, start mode 2, stop mode 1 and stop mode 2, a fixed positive or negative voltage is applied to the motor.

This voltage can be programmed as a percentage of the maximum possible voltage, via register 6, to limit current drain during start and stop.

The following power limits are possible:

- 100% (no power limit), 75%, 50% or 37% of maximum.

7.15.3 LOOP CHARACTERISTICS

The gain and crossover frequencies of the motor control loop can be programmed via decoder registers 4 and 5. The following parameter values are possible:

- Gains: 3.2, 4.0, 6.4, 8.0, 12.8, 16, 25.6 and 32
- Crossover frequency $f_4$: 0.5 × n Hz, 0.7 × n Hz, 1.4 × n Hz and 2.8 × n Hz
- Crossover frequency $f_3$: 0.85 × n Hz, 1.71 × n Hz and 3.42 × n Hz.

It should be noted that the crossover frequencies $f_3$ and $f_4$ are scaled with the overspeed factor ‘n’ whereas the gains are not.

7.15.4 FIFO OVERFLOW

If FIFO overflow occurs during Play mode (e.g. as a result of motor rotational shock), the FIFO will be automatically reset to 50% and the audio interpolator will conceal as much as possible to minimize the effect of data loss.

**Table 12** Operating modes

| MODE | DESCRIPTION |
|---|---|
| Start mode 1 | The disc is accelerated by applying a positive voltage to the spindle motor. No decisions are involved and the PLL is reset. No disc speed information is available for the microcontroller. |
| Start mode 2 | The disc is accelerated as in start mode 1, however the PLL will monitor the disc speed. When the disc reaches 75% of its nominal speed, the controller will switch to jump mode. The motor status signals selectable via register 2 are valid. |
| Jump mode | Motor servo enabled but FIFO kept reset at 50%, integrator is held. The audio is muted but it is possible to read the subcode. It should be noted that in the CD-ROM modes the data, on EBU and the $I^2S$-bus, is not muted. |
| Jump mode 1 | Similar to jump mode but motor integrator is kept at zero. It is used for long jumps where there is a large change in disc speed. |
| Play mode | FIFO released after resetting to 50% and the audio mute is released. |
| Stop mode 1 | Disc is braked by applying a negative voltage to the motor; no decisions are involved. |
| Stop mode 2 | The disc is braked as in stop mode 1 but the PLL will monitor the disc speed. As soon as the disc reaches 12% (or 6%, depending on the programmed brake percentage, via register E) of its nominal speed, the MOTSTOP status signal will go HIGH and switch the motor servo to off mode. |
| Off mode | Motor not steered. |

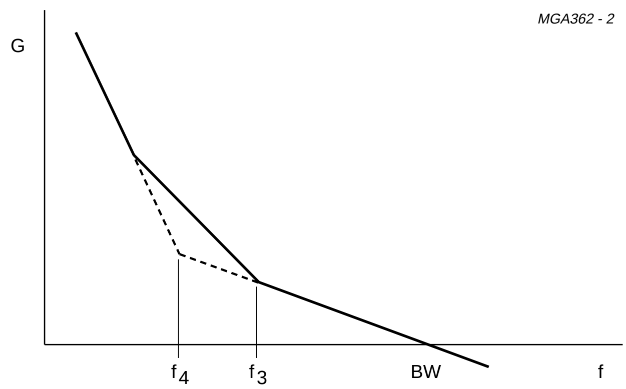



Fig.20 Motor servo mode diagram.

### 7.16 Servo part

#### 7.16.1 DIODE SIGNAL PROCESSING

The photo detector in conventional two-stage three-beam Compact Disc systems normally contains six discrete diodes. Four of these diodes (three for single foucault systems) carry the Central Aperture signal (CA) while the other two diodes (satellite diodes) carry the radial tracking information. The CA signals are summed into an HF signal for the decoder function and are also differentiated (after analog-to-digital conversion) to produce the low frequency focus control signals.

The low frequency content of the six (five if single Foucault) photo diode inputs are converted to digital Pulse Density Modulated (PDM) bitstreams by six Sigma-delta ADCs. These support a range of OPUs by interfacing to Voltage mode mechanisms and by having 16 selectable gain ranges in two sets, one set for D1-to-D4 and the other for R1 and R2.

**Table 13** Shadow register settings to control diode voltage ranges

| SHADEN BITS | SHADOW REGISTER | ADDRESS | DATA | VOLTAGE (mV) | INITIAL |
|---|---|---|---|---|---|
| 01 (bank 1) | A signal magnitude control for diodes D1 to D4 (LF only) | 1010 | 0000 | 20 | – |
| | | | 0001 | 25 | – |
| | | | 0010 | 30 | – |
| | | | 0011 | 40 | – |
| | | | 0100 | 60 | – |
| | | | 0101 | 75 | – |
| | | | 0110 | 100 | – |
| | | | 0111 | 120 | – |
| | | | 1000 | 150 | – |
| | | | 1001 | 200 | – |
| | | | 1010 | 270 | – |
| | | | 1011 | 350 | – |
| | | | 1100 | 450 | – |
| | | | 1101 | 600 | – |
| | | | 1110 | 720 | – |
| | | | 1111 | 960 | reset |

| SHADEN BITS | SHADOW REGISTER | ADDRESS | DATA | VOLTAGE (mV) | INITIAL |
|---|---|---|---|---|---|
| 01 (bank 1) | C signal magnitude control for diodes R1 and R2 (LF only) | 1100 | 0000 | 20 | – |
| | | | 0001 | 25 | – |
| | | | 0010 | 30 | – |
| | | | 0011 | 40 | – |
| | | | 0100 | 60 | – |
| | | | 0101 | 75 | – |
| | | | 0110 | 100 | – |
| | | | 0111 | 120 | – |
| | | | 1000 | 150 | – |
| | | | 1001 | 200 | – |
| | | | 1010 | 270 | – |
| | | | 1011 | 350 | – |
| | | | 1100 | 450 | – |
| | | | 1101 | 600 | – |
| | | | 1110 | 720 | – |
| | | | 1111 | 960 | reset |

#### 7.16.2 SIGNAL CONDITIONING

The digital codes retrieved from the ADCs are applied to logic circuitry to obtain the various control signals. The signals from the central aperture diodes are processed to obtain a normalised focus error signal:

$$FE_n = \frac{D1 - D2}{D1 + D2} - \frac{D3 - D4}{D3 + D4}$$

Where the detector set-up is assumed to be as shown in Fig.21.

In the event of single Foucault focusing method, the signal conditioning can be switched under software control such that the signal processing is as follows:

$$FE_n = 2 \times \frac{D1 - D2}{D1 + D2}$$

The error signal, $FE_n$, is further processed by a Proportional Integral and Differential (PID) filter section.

A Focus OK (FOK) flag is generated by the central aperture signal and an adjustable reference level. This signal is used to provide extra protection for the Track-Loss (TL) generation, the focus start-up procedure and the dropout detection.

The radial or tracking error signal is generated by the satellite detector signals R1 and R2. The radial error signal can be formulated as follows:

$RE_s$ = (R1 – R2) × re_gain + (R1 + R2) × re_offset.

Where the index ‘s’ indicates the automatic scaling operation which is performed on the radial error signal. This scaling is necessary to avoid non-optimum dynamic range usage in the digital representation and reduces the radial bandwidth spread. Furthermore, the radial error signal will be made free from offset during start-up of the disc.

The four signals from the central aperture detectors, together with the satellite detector signals generate a Track Position signal (TPI) which can be formulated as follows:

TPI = sign [(D1 + D2 + D3 + D4) – (R1 + R2) × sum_gain]

Where the weighting factor sum_gain is generated internally by the SAA7824 during initialization.

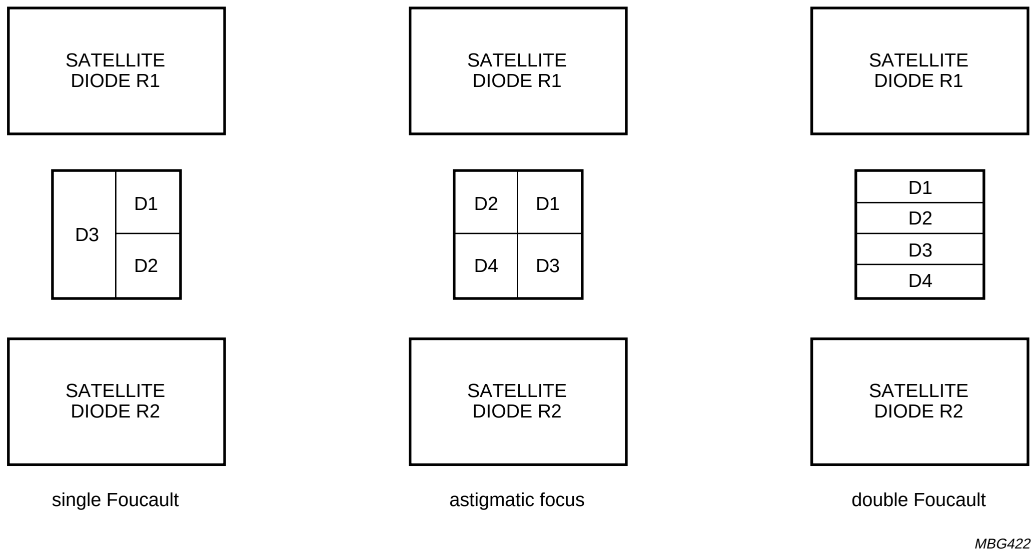



Fig.21 Detector arrangement.

### 7.16.3 FOCUS SERVO SYSTEM

#### *7.16.3.1 Focus start-up*

Five initially loaded coefficients influence the start-up behaviour of the focus controller. The automatically generated triangular voltage can be influenced by 3 parameters; for height (ramp_height) and DC offset (ramp_offset) of the triangle and its steepness (ramp_incr).

For protection against false focus point detections two parameters are available which are an absolute level on the CA signal (CA_start) and a level on the $FE_n$ signal (FE_start). When this CA level is reached the FOK signal becomes true.

If the FOK signal is true and the level on the $FE_n$ signal is reached, the focus PID is enabled to switch-on when the next zero crossing is detected in the $FE_n$ signal.

#### *7.16.3.2 Focus position control loop*

The focus control loop contains a digital PID controller which has 5 parameters that are available to the user. These coefficients influence the integrating (foc_int), proportional (foc_lead_length, part of foc_parm3) and differentiating (foc_pole_lead, part of foc_parm1) action of the PID and a digital low-pass filter (foc_pole_noise, part of foc_parm2) following the PID. The fifth coefficient foc_gain influences the loop gain.

#### *7.16.3.3 Dropout detection*

This detector can be influenced by one parameter (CA_drop). The FOK signal will become false and the integrator of the PID will hold if the CA signal drops below this programmable absolute CA level. When the FOK signal becomes false it is assumed, initially, to be caused by a black dot.

#### *7.16.3.4 Focus loss detection and fast restart*

Whenever FOK is false for longer than approximately 3 ms, it is assumed that the focus point is lost. A fast restart procedure is initiated which is capable of restarting the focus loop within 200 to 300 ms depending on the programmed coefficients of the microcontroller.

*7.16.3.5 Focus loop gain switching*

The gain of the focus control loop (foc_gain) can be multiplied by a factor of 2 or divided by a factor of 2 during normal operation. The integrator value of the PID is corrected accordingly. The differentiating (foc_pole_lead) action of the PID can be switched at the same time as the gain switching is performed.

*7.16.3.6 Focus automatic gain control loop*

The loop gain of the focus control loop can be corrected automatically to eliminate tolerances in the focus loop. This gain control injects a signal into the loop which is used to correct the loop gain. Since this decreases the optimum performance, the gain control should only be activated for a short time (for example, when starting a new disc).

### 7.16.4 RADIAL SERVO SYSTEM

*7.16.4.1 Level initialization*

During start-up an automatic adjustment procedure is activated to set the values of the radial error gain (re_gain), offset (re_offset) and satellite sum gain (sum_gain) for TPI level generation. The initialization procedure runs in a radial open loop situation and is ≤300 ms. This start-up time period may coincide with the last part of the motor start-up time period:

- Automatic gain adjustment: as a result of this initialization the amplitude of the RE signal is adjusted to within ±10% around the nominal RE amplitude
- Offset adjustment: the additional offset in RE due to the limited accuracy of the start-up procedure is less than ±50 nm
- TPI level generation: the accuracy of the initialization procedure is such that the duty factor range of TPI becomes 0.4 < duty factor < 0.6 (default duty factor = TPI HIGH/TPI period).

*7.16.4.2 Sledge control*

The microcontroller can move the sledge in both directions via the steer sledge command.

*7.16.4.3 Tracking control*

The actuator is controlled using a PID loop filter with user defined coefficients and gain. For stable operation between the tracks, the S-curve is extended over 75% of the track. On request from the microcontroller, S-curve extension over 2.25 tracks is used, automatically changing to access control when exceeding those 2.25 tracks.

Both modes of S-curve extension make use of a track-count mechanism. In this mode, track counting results in an ‘automatic return-to-zero track’, to avoid major disturbances in the audio output and providing improved shock resistance. The sledge is continuously controlled, or provided with step pulses to reduce power consumption using the filtered value of the radial PID output. Alternatively, the microcontroller can read the average voltage on the radial actuator and provide the sledge with step pulses to reduce power consumption. Filter coefficients of the continuous sledge control can be preset by the user.

*7.16.4.4 Access*

The access procedure is divided into two different modes (see Table 14), depending on the requested jump size.

**Table 14** Access modes

| ACCESS TYPE | JUMP SIZE(1) | ACCESS SPEED |
|---|---|---|
| Actuator jump | 1 – brake_distance | decreasing velocity |
| Sledge jump | brake_distance –32768 | maximum power to sledge(1) |

**Note**

1. The microcontroller can be preset.

The access procedure makes use of a track counting mechanism, a velocity signal based on a fixed number of tracks passed within a fixed time interval, a velocity set point calculated from the number of tracks to go and a user programmable parameter indicating the maximum sledge performance.

If the number of tracks remaining is greater than the brake_distance then the sledge jump mode should be activated or, the actuator jump should be performed. The requested jump size together with the required sledge breaking distance at maximum access speed defines the brake_distance value.

During the actuator jump mode, velocity control with a PI controller is used for the actuator. The sledge is then continuously controlled using the filtered value of the radial PID output. All filter parameters (for actuator and sledge) are user programmable.

In the sledge jump mode maximum power (user programmable) is applied to the sledge in the correct direction while the actuator becomes idle (the content of the actuator integrator leaks to zero just after the sledge jump mode is initiated). The actuator can be electronically damped during sledge jump. The gain of the damping loop is controlled via the hold_mult parameter.

The fast track jumping circuitry can be enabled or disabled via the xtra_preset parameter.

#### *7.16.4.5 Radial automatic gain control loop*

The loop gain of the radial control loop can be corrected automatically to eliminate tolerances in the radial loop. This gain control injects a signal into the loop which is used to correct the loop gain. Since this decreases the optimum performance, the gain control should only be activated for a short time (for example, when starting a new disc).

This gain control differs from the level initialization. The level initialization should be performed first. The disadvantage of using the level initialization without the gain control is that only tolerances from the front-end are reduced.

### 7.16.5 OFF-TRACK COUNTING

The Track Position signal (TPI) is a flag which is used to indicate whether the radial spot is positioned on the track, with a margin of ±0.25 of the track pitch. In combination with the Radial Polarity flag (RP) the relative spot position over the tracks can be determined.

These signals can have uncertainties caused by:

- Disc defects such as scratches and fingerprints
- The HF information on the disc, which is considered as noise by the detector signals.

In order to determine the spot position with sufficient accuracy, extra conditions are necessary to generate a Track Loss signal (TL) and an off-track counter value. These extra conditions influence the maximum speed and this implies that, internally, one of the following three counting states is selected:

1. Protected state: used in normal play situations. A good protection against false detection caused by disc defects is important in this state.
2. Slow counting state: used in low velocity track jump situations. In this state a fast response is important rather than the protection against disc defects (if the phase relationship between TL and RP of 0.5π radians is affected too much, the direction cannot then be determined accurately).
3. Fast counting state: used in high velocity track jump situations. Highest obtainable velocity is the most important feature in this state.

### 7.16.6 TRACK COUNTING MODES

Fast counting mode is auto-selected for a track crossing speed above 1200 tracks/s. In this case the off-track counting decrements occur only for effect of the RP signal, and the direction of the jump is already known because the Slow counting mode occurs before going into Fast counting mode.

When the Slow counting mode is selected, the maximum track crossing speed that can be reached is 12 kHz (providing that the maximum value for rad_pole_lead is used). In this case the direction of the jump is given by the phase shift between RP and TL (+90 degrees for outward jumps, –90 degrees for inward jumps). The number of pulses in the TL signal gives the number of tracks crossed.

When the Fast counting mode is enabled, whenever the track crossing speed goes below 12 kHz, the counting mode is automatically changed to Slow.

### 7.16.7 DEFECT DETECTION

A defect detection circuit is incorporated into the SAA7824. If a defect is detected, the radial and focus error signals may be zeroed, resulting in better playability. The defect detector can be switched off, applied only to focus control or applied to both focus and radial controls under software control (part of foc_parm1).

The defect detector (see Fig 22) has programmable set points selectable by the parameter defect_parm.

### 7.16.8 OFF-TRACK DETECTION

During active radial tracking, off-track detection has been realised by continuously monitoring the off-track counter value. The off-track flag becomes valid whenever the off-track counter value is not equal to zero. Depending on the type of extended S-curve, the off-track counter is reset after 0.75 extend or at the original track in the 2.25 track extend mode.

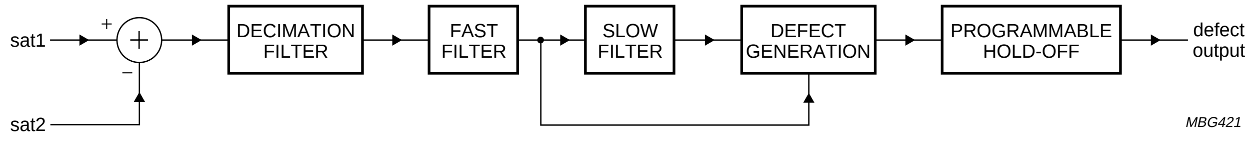



Fig.22 Block diagram of the defect detector.

### 7.16.9 HIGH-LEVEL FEATURES

#### *7.16.9.1 Interrupt mechanism and STATUS pin*

The STATUS pin is an output which can be configured by decoder register 7 and new shadow register C (bank 3) for one of three different modes of operation. These are:

- Output the interrupt signal generated by the servo part (it should be noted that the selection of this mode will override all other modes)
- Output the decoder status bit (active LOW) selected by decoder register 2 (only available in 4-wire bus mode)
- Output DC offset information (it should be noted that this mode is used in conjunction with the decoder status mode; see Section 7.5).

Eight signals from the interrupt status register are selectable from the servo part via the interrupt_mask parameter. The interrupt is reset by sending the read high-level status command. The 8 signals are as follows:

- Focus lost: dropout of longer than 3 ms
- Subcode ready
- Subcode absolute seconds changed
- Subcode discontinuity detected: new subcode time before previous subcode time, or more than 10 frames later than previous subcode time
- Radial error: during radial on-track, no new subcode frame occurs within the time defined by the ‘playwatchtime’ parameter; during radial jump, less than 4 tracks have been crossed during the time defined by the ‘jumpwatchtime’ parameter
- Autosequencer state change
- Autosequencer error
- Subcode interface blocked: the internal decoder interface is being used.

It should be noted that if the STATUS pin is configured to output decoder status information [decoder register 7 = XX10 and new shadow register C (bank 3) = X00X] and either the microcontroller writes a different value to decoder register 2 or the decoder interface is enabled then the STATUS output will change.

#### *7.16.9.2 Decoder interface*

The decoder interface allows decoder and shadow registers to be programmed and subcode Q-channel data to be read via servo commands. The interface is enabled or disabled by the preset latch command (and the xtra_preset parameter).

#### *7.16.9.3 Automatic error handling*

Three Watchdogs are present:

- Focus: detects focus dropout of longer than 3 ms, sets focus lost interrupt, switches off radial and sledge servos and disables the drive-to-disc motor
- Radial play: started when radial servo is in on-track mode and a first subcode frame is found; detects when the maximum time between two subcode frames exceeds the time set by the playwatchtime parameter; it then sets the radial error interrupt, switches radial and sledge servos off and puts the disc motor into jump mode
- Radial jump: active when radial servo is in long jump or short jump modes; detects when the off-track counter value decreases by less than 4 tracks between two readings (the time interval is set by the jumpwatchtime parameter); it then sets the radial jump error, switches radial and sledge servos off to cancel jump.

The focus Watchdog is always active, the radial Watchdogs are selectable via the radcontrol parameter.

*7.16.9.4 Automatic sequencers and timer interrupts*

Two automatic sequencers are implemented (and must be initialized after Power-on):

- Auto-start sequencer: controls the start-up of focus, radial and motor
- Auto-stop sequencer: brakes the disc and shuts down the servos.

When the automatic sequencers are not used it is possible to generate timer interrupts, defined by the time_parameter coefficient.

*7.16.9.5 High-level status*

The read high-level status command can be used to obtain the interrupt, decoder, autosequencer status registers and the motor start time. Use of the read high-level status command clears the interrupt status register, and re-enables the subcode read via a servo command.

### 7.16.10 DRIVER INTERFACE

The control signals (pins RA, FO and SL) for the mechanism actuators are pulse density modulated. The modulating frequency can be set to either 1.0584 or 2.1168 MHz; controlled via the xtra_preset parameter. An analog representation of the output signals can be achieved by connecting a 1st-order low-pass filter to the outputs.

During reset (i.e. $\overline{\text{RESET}}$ pin is held LOW) the RA, FO and SL pins are high-impedance. At all other times, when the laser is switched off, the RA and FO pins output a 2 MHz 50% duty factor signal.

### 7.16.11 LASER INTERFACE

The laser diode pre-amplifier function is built into the SAA7824 and is illustrated in Fig.24. The current can be regulated, up to 120 mA in four steps ranging from 58% up to full power. New shadow register A (bank 2) and new shadow register 3 (bank 3) are used to select the step values.

The voltage derived from the monitor diode is maintained at a steady state by the laser drive circuitry, regulating the current through the laser diode. The type of monitor diode being used (150 mV or 180 mV) must be selected by new shadow register 7 (bank 2) (reset state = 150 mV).

The laser can be switched on or off by the xtra_preset parameter; it is automatically driven if the focus control loop is active.

### 7.17 Microcontroller interface

Communication on the microcontroller interface can be set-up in three different modes:

- 4-wire bus mode: where:
  - SCL = serial clock
  - SDA = serial data
  - RAB = R/$\overline{W}$ control and data strobe (active HIGH) for writing to decoder registers 0 to F, reading status bit selected via decoder register 2 and reading Q-channel subcode
  - SILD = $\overline{R}$/W control and data strobe (active LOW) for servo commands
- 3-wire bus mode: where:
  - SCL = serial clock
  - SDA = serial data
  - RAB = not used, pulled LOW
  - SILD = $\overline{R}$/W control and data strobe (active LOW) for servo commands
- $I^2C$-bus mode: $I^2C$-bus protocol where the SAA7824 behaves as slave device, activated by setting RAB = HIGH and SILD = LOW where:
  - $I^2C$-bus slave address (write mode) = 30H
  - $I^2C$-bus slave address (read mode) = 31H
  - Maximum data transfer rate = 400 kbits/s.

It should be noted that when using the $I^2C$-bus mode, only servo commands can be used. Therefore, writing to decoder registers 0 to F, reading decoder status and reading Q-channel subcode data must be performed by servo commands.

The 3-wire mode is very similar to the 4-wire mode, except that all communication to the decoder is via the servo.

Communication to the servo uses the same hardware protocol and timing as the 4-wire mode.

Extra servo commands exist for read and write access to the decoder via the internal decoder interface. The internal interface must be enabled by using the xtra_preset command. RAB is not used and must be tied LOW; see Fig.23

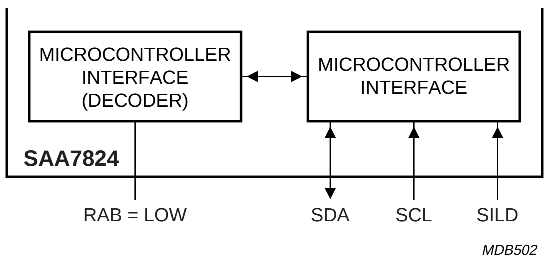



Fig.23 Microcontroller interface for the 3-wire mode.

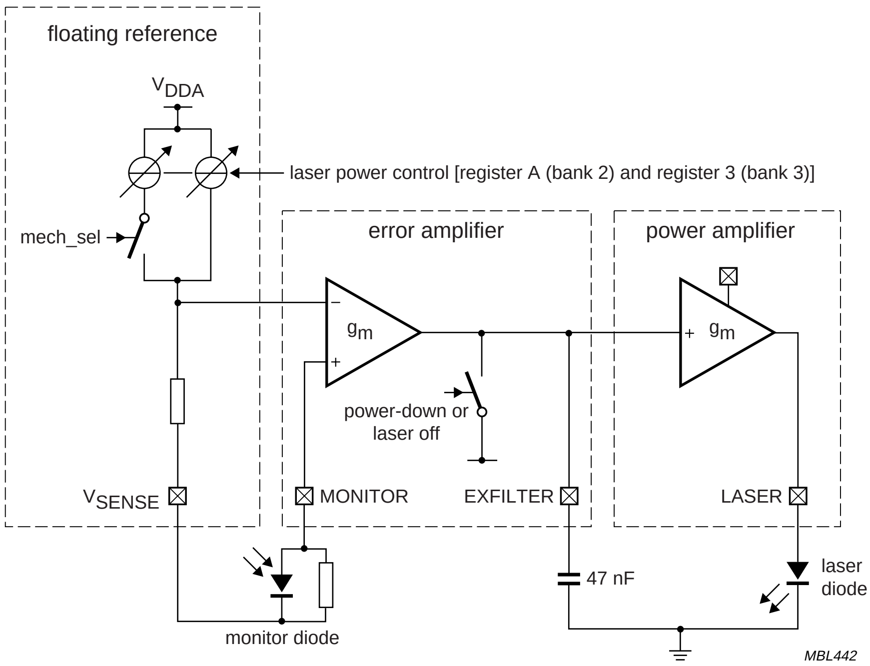



Fig.24 Simplified block diagram of the laser driver.

#### 7.17.1 MICROCONTROLLER INTERFACE (4-WIRE BUS MODE)

##### *7.17.1.1 Writing data to registers 0 to F*

The sixteen 4-bit programmable configuration registers, 0 to F (see Table 15), can be written to via the microcontroller interface using the protocol shown in Fig.25. It should be noted that SILD must be held HIGH; A3 to A0 identifies the register number and D3 to D0 is the data. The data is latched into the register on the LOW-to-HIGH transition of RAB.

##### *7.17.1.2 Writing repeated data to registers 0 to F*

The same data can be repeated several times (e.g. for a fade function) by applying extra RAB pulses as shown in Fig.26. It should be noted that SCL must stay HIGH between RAB pulses.

##### *7.17.1.3 Multiple writes to the new shadow registers*

Some of the new shadow registers are a multiple of four bits in length and require a number of write operations to fill them up; see Section 7.17.5. They must be completely filled before writing to another register, otherwise unpredictable behaviour may result.

The protocol for writing to these registers is exactly the same as the decoder registers; see Fig.25. The write command must be executed multiple times with the same address content. The first four bits of data in a sequence of write commands represent the most significant nibble of the register, while the last four represent the least significant nibble. The data content can change from one write to the next without consequence.

##### *7.17.1.4 Reading decoder status information on SDA*

There are several internal status signals, selected via register 2, which can be made available on the SDA line:

- SUBQREADY-I: LOW if new subcode word is ready in Q-channel register
- MOTSTART1: HIGH if motor is turning at 75% or more of nominal speed
- MOTSTART2: HIGH if motor is turning at 50% or more of nominal speed
- MOTSTOP: HIGH if motor is turning at 12% or less of nominal speed; can be set to indicate 6% or less (instead of 12% or less) via register E
- PLL lock: HIGH if sync coincidence signals are found
- V1: follows input on pin V1
- V2: follows input on pin V2
- MOTOR-OV: HIGH if the motor servo output stage saturates.

The status read protocol is illustrated in Fig.27. It should be noted that SILD must be held HIGH.

##### *7.17.1.5 Reading Q-channel subcode*

To read the Q-channel subcode direct in the 4-wire bus mode, the SUBQREADY-I signal should be selected as the status signal. The subcode read protocol is illustrated in Fig.28.

It should be noted that SILD must be held HIGH; after subcode read starts, the microcontroller may take as long as it wants to terminate the read operation. When enough subcode has been read (1 to 96 bits), the reading can be terminated by pulling RAB LOW.

Alternatively, the Q-channel subcode can be read using a servo command as follows:

- Use the read high-level status command to monitor the subcode ready signal
- Send the read subcode command and read the required number of bytes (up to 12)
- Send the read high-level status command; to re-enable the decoder interface.

##### *7.17.1.6 Behaviour of the SUBQREADY-I signal*

When the CRC of the Q-channel word is good, and no subcode is being read, the SUBQREADY-I status signal will react as illustrated in Fig.29. When the CRC is good and the subcode is being read, the timing in Fig.30 applies.

If $t_1$ (SUBQREADY-I status LOW to end of subcode read) is below 2.6/n ms, then $t_2$ = 13.1/n ms (i.e. the microcontroller can read all subcode frames if it completes the read operation within 2.6/n ms after the subcode is ready). If these criteria are not met, it is only possible to guarantee that $t_3$ will be below 26.2/n ms (approximately).

If subcode frames with failed CRCs are present, the $t_2$ and $t_3$ times will be increased by 13.1/n ms for each defective subcode frame.

It should be noted that in the lock-to-disc mode ‘n’ is replaced by ‘d’, which is the disc speed factor.

#### 7.17.1.7 *Write servo commands*

A write data command is used to transfer data (a number of bytes) from the microcontroller, using the protocol illustrated in Fig.31. The first of these bytes is the command byte and the following are data bytes; the number (between 1 and 7) depends on the command byte.

It should be noted that RAB must be held LOW; the command or data is interpreted by the SAA7824 after the HIGH-to-LOW transition of SILD; there must be a minimum time of 70 µs between SILD pulses.

#### 7.17.1.8 *Writing repeated data in servo commands*

The same data byte can be repeated by applying extra SILD pulses as illustrated in Fig.32. SCL must be HIGH between the SILD pulses.

#### 7.17.1.9 *Read servo commands*

A read data command is used to transfer data (status information) to the microcontroller, using the protocol shown in Fig.33. The first byte written determines the type of command. After this byte a variable number of bytes can be read. It should be noted that RAB must be held LOW; after the end of the command byte (LOW-to-HIGH transition on SILD) there must be a delay of 70 µs before data can be read (i.e. the next HIGH-to-LOW transition on SILD) and there must be a minimum time of 70 µs between SILD pulses.

### 7.17.2 MICROCONTROLLER INTERFACE ($I^2C$-BUS MODE)

Bytes are transferred over the interface in groups (i.e. servo commands) of which there are two types: write data commands and read data commands.

The sequence for a write data command (that requires 3 data bytes) is as follows:

1. Send START condition.
2. Send address 30H (write).
3. Write command byte.
4. Write data byte 1.
5. Write data byte 2.
6. Write data byte 3.
7. Send STOP condition.

It should be noted that more than one command can be sent in one write sequence.

The sequence for a read data command (that reads 2 data bytes) is as follows:

1. Send START condition.
2. Send address 30H (write).
3. Write command byte.
4. Send STOP condition.
5. Send START condition.
6. Send address 31H (read).
7. Read data byte 1.
8. Read data byte 2.
9. Send STOP condition.

It should be noted that the timing constraints specified for the read and write servo commands must still be adhered to.

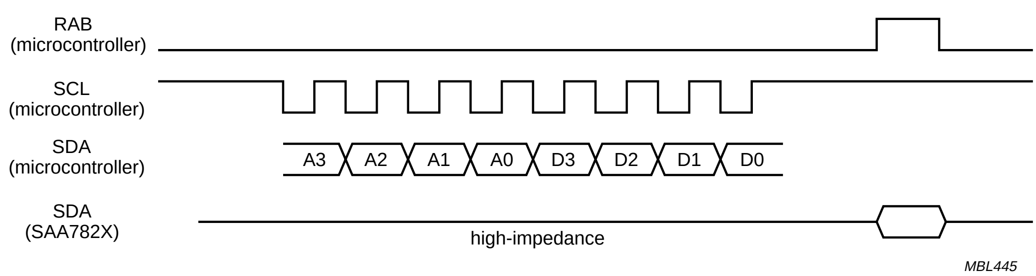



Fig.25 Microcontroller write protocol for registers 0 to F.

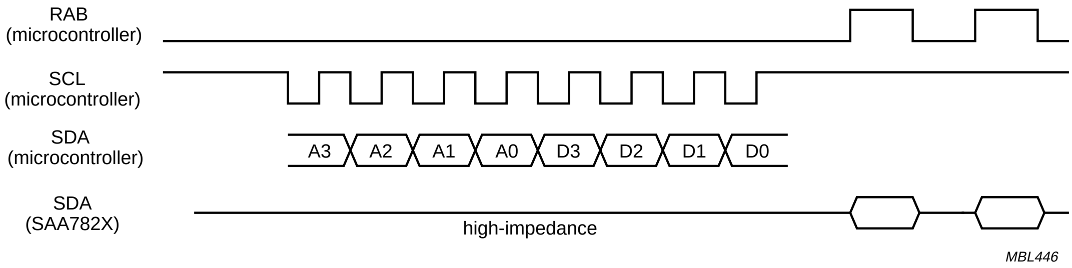



Fig.26 Microcontroller write protocol for registers 0 to F (repeat mode).

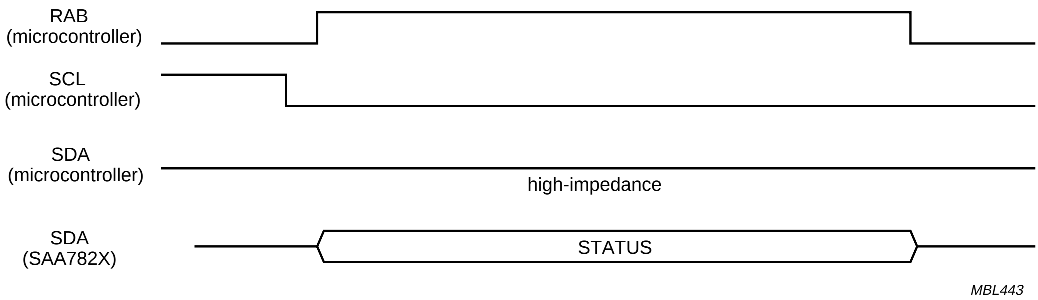



Fig.27 Microcontroller read protocol for decoder status on SDA.

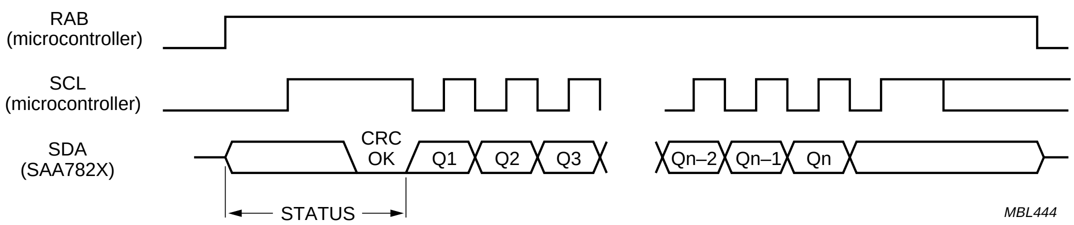



Fig.28 Microcontroller protocol for reading Q-channel subcode.

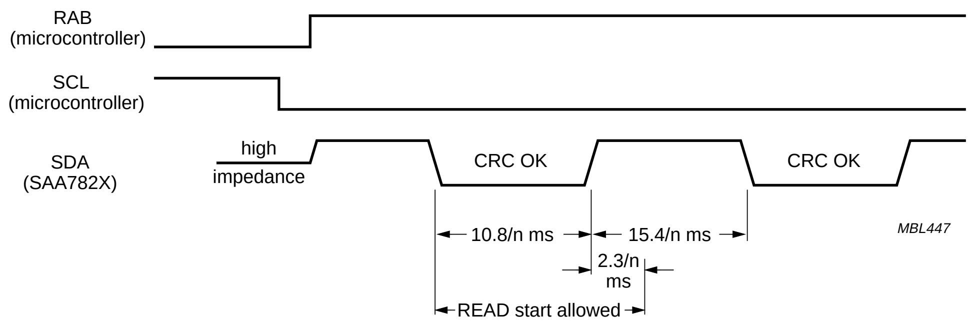



Fig.29 SUBQREADY-I status timing when no subcode is read.

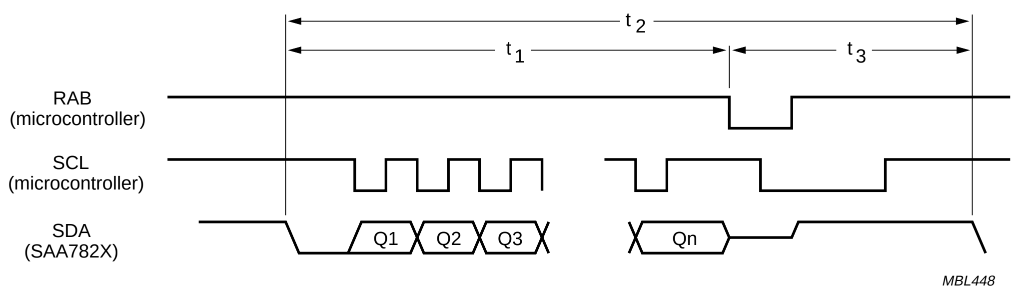



Fig.30 SUBQREADY-I status timing when subcode is read.

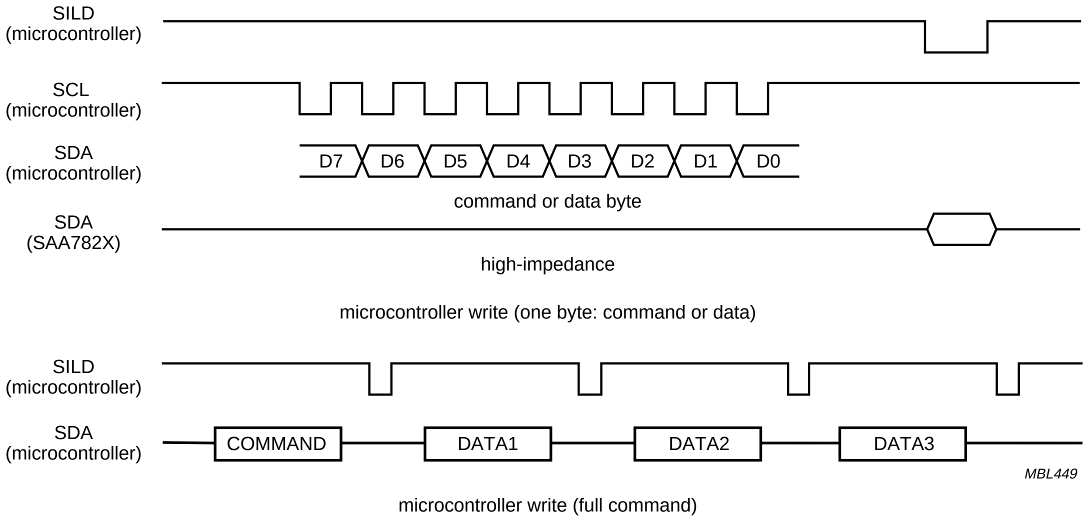



Fig.31 Microcontroller protocol for write servo commands.

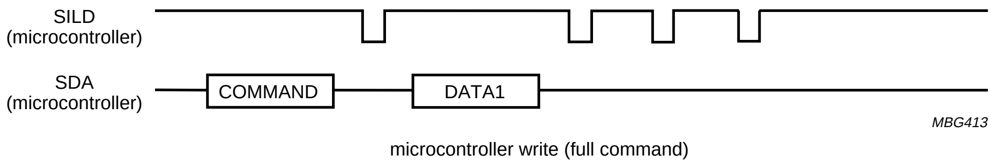



Fig.32 Microcontroller protocol for repeated data in write servo commands.

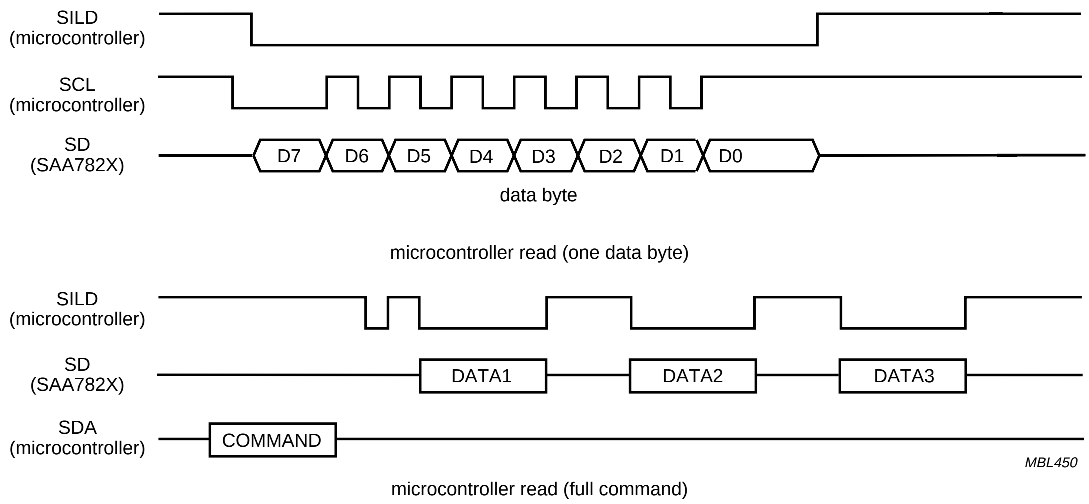



Fig.33 Microcontroller protocol for read servo commands.

#### 7.17.3 DECODER AND SHADOW REGISTERS

To maintain compatibility with the SAA732x series, decoder registers 0 to F and the shadow registers are largely unchanged. However, to control the extra functionality of SAA7824, the shadow registers have been extended to include new shadow registers.

All shadow registers are accessed by using the two LSBs (bits 0 and 1) of decoder register F. These bits are called SHADEN1 and SHADEN2 respectively. These bits are decoded according to Table 15.

This two bit encoding allows the use of three shadow register banks; bank 1 (SAA732X shadow registers), and banks 2 and 3 (new shadow registers). Only the four addresses 3, 7, A and C are implemented in any one bank. Any other addresses sent while accessing any of the shadow register banks are invalid and have no effect.

When SHADEN1 and SHADEN2 are both set to logic 0 (decoder register F set to XX00) all subsequent addresses are decoded by the main decoder registers again.

Access to decoder register F is always enabled so that SHADEN1 and SHADEN2 can be set or reset as required.

The SHADEN bits and subsequent shadow registers are programmed identically to the main decoder registers, i.e. they can be directly programmed when using the SAA7824 in 4-wire mode or programmed via the servo interface when using 3-wire or I$^2$C-bus modes. The main decoder registers are given in Table 16 and the shadow registers in Table 18. Details of the new shadow registers can be found in Tables 19 to 22.

**Table 15** Shadow register accessibility

| SHADEN2 | SHADEN1 | FUNCTION | INITIAL |
|---|---|---|---|
| 0 | 0 | access decoder registers 0 to F | reset |
| 0 | 1 | access SAA732X shadow registers (bank 1) | – |
| 1 | 0 | access new shadow registers (bank 2) | – |
| 1 | 1 | access new shadow registers (bank 3) | – |

7.17.4 SUMMARY OF FUNCTIONS CONTROLLED BY DECODER REGISTERS 0 TO F

**Table 16** Registers 0 to F

| REGISTER | ADDRESS | DATA | FUNCTION | INITIAL(1) |
|---|---|---|---|---|
| 0 (Fade and attenuation) | 0000 | X000 | mute | reset |
| | | X010 | attenuate | – |
| | | X001 | full-scale | – |
| | | X100 | step-down | – |
| | | X101 | step-up | – |
| 0 EBU mute (for M1 version only) | | 0XXX | EBU mute inactive | reset |
| | | 1XXX | EBU mute active | – |
| 1 (Motor mode) | 0001 | X000 | motor off mode | reset |
| | | X001 | motor stop mode 1 | – |
| | | X010 | motor stop mode 2 | – |
| | | X011 | motor start mode 1 | – |
| | | X100 | motor start mode 2 | – |
| | | X101 | motor jump mode | – |
| | | X111 | motor play mode | – |
| | | X110 | motor jump mode 1 | – |
| | | 1XXX | anti-windup active | – |
| | | 0XXX | anti-windup off | reset |
| 2 (Status control) | 0010 | 0000 | status = SUBQREADY-I | reset |
| | | 0001 | status = MOTSTART1 | – |
| | | 0010 | status = MOTSTART2 | – |
| | | 0011 | status = MOTSTOP | – |
| | | 0100 | status = PLL lock | – |
| | | 0101 | status = V1 | – |
| | | 0110 | status = V2 | – |
| | | 0111 | status = MOTOR-OV | – |
| unavailable via the I$^2$C-bus or 3-wire mode | | 1000 | status = FIFO overflow | – |
| | | 1001 | status = shock detect | – |
| | | 1010 | status = latched shock detect | – |
| | | 1011 | status = latched shock detect reset | – |

| REGISTER | ADDRESS | DATA | FUNCTION | INITIAL(1) |
|---|---|---|---|---|
| 3 (DAC output) | 0011 | 1010 | $I^2S$-bus; CD-ROM mode | – |
| | | 1011 | EIAJ; CD-ROM mode | – |
| | | 1100 | $I^2S$-bus; 18-bit; $4f_s$ mode | reset |
| | | 1111 | $I^2S$-bus; 18-bit; $2f_s$ mode | – |
| | | 1110 | $I^2S$-bus; 16-bit; $f_s$ mode | – |
| | | 0000 | EIAJ; 16-bit; $4f_s$ | – |
| | | 0011 | EIAJ; 16-bit; $2f_s$ | – |
| | | 0010 | EIAJ; 16-bit; $f_s$ | – |
| | | 0100 | EIAJ; 18-bit; $4f_s$ | – |
| | | 0111 | EIAJ; 18-bit; $2f_s$ | – |
| | | 0110 | EIAJ; 18-bit; $f_s$ | – |
| 4 (Motor gain) | 0100 | 0000 | motor gain G = 3.2 | reset |
| | | 0001 | motor gain G = 4.0 | – |
| | | 0010 | motor gain G = 6.4 | – |
| | | 0011 | motor gain G = 8.0 | – |
| | | 0100 | motor gain G = 12.8 | – |
| | | 0101 | motor gain G = 16.0 | – |
| | | 0110 | motor gain G = 25.6 | – |
| | | 0111 | motor gain G = 32.0 | – |
| 5 (Motor bandwidth) | 0101 | XX00 | motor $f_4 = 0.5 \times n$ Hz | reset |
| | | XX01 | motor $f_4 = 0.7 \times n$ Hz | – |
| | | XX10 | motor $f_4 = 1.4 \times n$ Hz | – |
| | | XX11 | motor $f_4 = 2.8 \times n$ Hz | – |
| | | 00XX | motor $f_3 = 0.85 \times n$ Hz | reset |
| | | 01XX | motor $f_3 = 1.71 \times n$ Hz | – |
| | | 10XX | motor $f_3 = 3.42 \times n$ Hz | – |
| 6 (Motor output configuration) | 0110 | XX00 | motor power maximum 37% | reset |
| | | XX01 | motor power maximum 50% | – |
| | | XX10 | motor power maximum 75% | – |
| | | XX11 | motor power maximum 100% | – |
| | | 00XX | MOTO1, MOTO2 pins 3-state | reset |
| | | 01XX | motor PWM mode | – |
| | | 10XX | motor PDM mode | – |
| | | 11XX | motor CDV mode | – |

| REGISTER | ADDRESS | DATA | FUNCTION | INITIAL[1] |
|---|---|---|---|---|
| 7 (DAC output and STATUS pin control) | 0111 | XX00 | interrupt signal from servo only at STATUS pin | reset |
| | | XX10 | status bit from decoder status register or DC offset information at STATUS pin [see also new shadow register C (bank 3)] | – |
| | | X0XX | DAC data normal value | reset |
| | | X1XX | DAC data inverted value | – |
| | | 0XXX | left channel first at DAC (WCLK normal) | reset |
| | | 1XXX | right channel first at DAC (WCLK inverted) | – |
| 8 (PLL loop filter bandwidth) | | | see Table 16 | – |
| 9 (PLL equalization) | 1001 | 0011 | PLL loop filter equalization | reset |
| | | 0001 | PLL 30 ns over-equalization | – |
| | | 0010 | PLL 15 ns over-equalization | – |
| | | 0100 | PLL 15 ns under-equalization | – |
| | | 0101 | PLL 30 ns under-equalization | – |
| A (EBU output) | 1010 | XX0X | EBU data before concealment | – |
| | | XX1X | EBU data after concealment and fade | reset |
| | | X0X0 | Level II clock accuracy (<1000 ppm) | reset |
| | | X0X1 | Level I clock accuracy (<50 ppm) | – |
| | | X1X0 | Level III clock accuracy (>1000 ppm) | – |
| | | X1X1 | EBU off - output LOW | – |
| | | 0XXX | flags in EBU off | reset |
| | | 1XXX | flags in EBU on | – |
| B (speed control) | 1011 | X000 | standby 1: ‘CD-STOP’ mode | reset |
| | | X010 | standby 2: ‘CD-PAUSE’ mode | – |
| | | X011 | operating mode | – |
| | | 00XX | single-speed mode | reset |
| | | 10XX | double-speed mode | – |
| C (versatile pins interface and KILL function) | 1100 | XXX1 | external off-track signal input at V1 | – |
| | | XXX0 | internal off-track signal used (V1 may be read via status) | reset |
| | | XX0X | stereo KILL | – |
| | | XX1X | mono KILL | reset |
| | | 00XX | V3 = 0 | reset |
| | | 01XX | V3 = 1 | – |
| EBU mute mode (for M1 version only) | | 0XXX | mute type = soft mute audio; only available at 1× speed | reset |
| | | 1XXX | mute type = ROM hard mute; available at 1×, 2× and 4× speed | – |

| REGISTER | ADDRESS | DATA | FUNCTION | INITIAL[1] |
|---|---|---|---|---|
| D (versatile pins interface) | 1101 | 0000 | 4-line motor (using V4 and V5) | – |
| | | XX01 | Q-to-W subcode at V4 | – |
| | | XX10 | V4 = 0 | – |
| | | XX11 | V4 = 1 | reset |
| | | 01XX | de-emphasis signal at V5, no internal de-emphasis filter | – |
| | | 10XX | V5 = 0 | – |
| | | 11XX | V5 = 1 | reset |
| E | 1110 | XXX0 | motor brakes to 12% | reset |
| | | XXX1 | motor brakes to 6% | – |
| | | XX0X | lock-to-disc mode disabled | reset |
| | | XX1X | lock-to-disc mode enabled | – |
| | | X0XX | audio features disabled | – |
| | | X1XX | audio features enabled | reset |
| | | 0XXX | quad-speed mode disabled | reset |
| | | 1XXX | quad-speed mode enabled | – |
| F (subcode interface and shadow register enable) | 1111 | X0XX | subcode interface off | reset |
| | | X1XX | subcode interface on | – |
| | | 0XXX | 4-wire subcode | reset |
| | | 1XXX | 3-wire subcode | – |
| | | XX00 | SHADEN bits = 00; shadow registers not enabled; addresses will be decoded by main decoder registers | reset |
| | | XX01 | SHADEN bits = 01; SAA732X shadow registers (bank 1) enabled; all subsequent addresses will be decoded by shadow register (bank 1), not decoder registers | – |
| | | XX10 | SHADEN bits = 10; new shadow registers (bank 2) enabled; all subsequent addresses will be decoded by shadow register (bank 2) | – |
| | | XX11 | SHADEN bits = 11; new shadow registers (bank 3) enabled; all subsequent addresses will be decoded by shadow register (bank 3) | – |

**Note**

1. The initial column shows the Power-on reset state.

**Table 17** Loop filter bandwidth

| REGISTER | ADDRESS | DATA | FUNCTION | | | INITIAL(1) |
|---|---|---|---|---|---|---|
| | | | LOOP BANDWIDTH (Hz) | INTERNAL BANDWIDTH (Hz) | LOW-PASS BANDWIDTH (Hz) | |
| 8 (PLL loop filter bandwidth) | 1000 | 0000 | 1640 × n | 525 × n | 8400 × n | – |
| | | 0001 | 3279 × n | 263 × n | 16800 × n | – |
| | | 0010 | 6560 × n | 131 × n | 33600 × n | – |
| | | 0100 | 1640 × n | 1050 × n | 8400 × n | – |
| | | 0101 | 3279 × n | 525 × n | 16800 × n | – |
| | | 0110 | 6560 × n | 263 × n | 33600 × n | – |
| | | 1000 | 1640 × n | 2101 × n | 8400 × n | – |
| | | 1001 | 3279 × n | 1050 × n | 16800 × n | reset |
| | | 1010 | 6560 × n | 525 × n | 33600 × n | – |
| | | 1100 | 1640 × n | 4200 × n | 8400 × n | – |
| | | 1101 | 3279 × n | 2101 × n | 16800 × n | – |
| | | 1110 | 6560 × n | 1050 × n | 33600 × n | – |

**Note**

1. The initial column shows the Power-on reset state.

#### 7.17.5 SUMMARY OF FUNCTIONS CONTROLLED BY SHADOW REGISTERS

**Table 18** Bank 1 shadow register settings (single write)

| SHADEN BITS | SHADOW REGISTER | ADDRESS | DATA | FUNCTION | INITIAL |
|---|---|---|---|---|---|
| 01 (bank 1) | 3 control of versatile and clock pins | 0011 | XX00 | select CLK4 on CLK4/12 output | reset |
| | | | XX01 | select CLK12 on CLK4/12 output | – |
| | | | X0XX | enable CLK16 output pin | reset |
| | | | X1XX | set CLK16 output pin to high-impedance | – |
| | | | 0XXX | set V3 output pin to high-impedance | reset |
| | | | 1XXX | enable V3 output pin | – |
| | 7 control of onboard DAC | 0111 | 0000 | use external DAC or route audio data back into onboard DAC (loopback mode) | reset |
| | | | 0010 | route audio data directly into onboard DAC (non-loopback mode) | – |
| | 7 EBU mute bypass control (for M1 version only) | | XXX0 | EBU mute function not bypassed | reset |
| | | | XXX1 | EBU mute function bypassed | – |

| SHADEN BITS | SHADOW REGISTER | ADDRESS | DATA | FUNCTION | INITIAL |
|---|---|---|---|---|---|
| 01 (bank 1) | A signal magnitude control for diodes D1 to D4 (LF only) | 1010 | 0000 | voltage mode: 20 mV | – |
| | | | 0001 | voltage mode: 25 mV | – |
| | | | 0010 | voltage mode: 30 mV | – |
| | | | 0011 | voltage mode: 40 mV | – |
| | | | 0100 | voltage mode: 60 mV | – |
| | | | 0101 | voltage mode: 75 mV | – |
| | | | 0110 | voltage mode: 100 mV | – |
| | | | 0111 | voltage mode: 120 mV | – |
| | | | 1000 | voltage mode: 150 mV | – |
| | | | 1001 | voltage mode: 200 mV | – |
| | | | 1010 | voltage mode: 270 mV | – |
| | | | 1011 | voltage mode: 350 mV | – |
| | | | 1100 | voltage mode: 450 mV | – |
| | | | 1101 | voltage mode: 600 mV | – |
| | | | 1110 | voltage mode: 720 mV | – |
| | | | 1111 | voltage mode: 960 mV | reset |
| 01 (bank 1) | C signal magnitude control for diodes R1 and R2 (LF only) | 1100 | 0000 | voltage mode: 20 mV | – |
| | | | 0001 | voltage mode: 25 mV | – |
| | | | 0010 | voltage mode: 30 mV | – |
| | | | 0011 | voltage mode: 40 mV | – |
| | | | 0100 | voltage mode: 60 mV | – |
| | | | 0101 | voltage mode: 75 mV | – |
| | | | 0110 | voltage mode: 100 mV | – |
| | | | 0111 | voltage mode: 120 mV | – |
| | | | 1000 | voltage mode: 150 mV | – |
| | | | 1001 | voltage mode: 200 mV | – |
| | | | 1010 | voltage mode: 270 mV | – |
| | | | 1011 | voltage mode: 350 mV | – |
| | | | 1100 | voltage mode: 450 mV | – |
| | | | 1101 | voltage mode: 600 mV | – |
| | | | 1110 | voltage mode: 720 mV | – |
| | | | 1111 | voltage mode: 960 mV | reset |

**Table 19** Bank 2 new shadow register settings (single write)

| SHADEN BITS | SHADOW REGISTER | ADDRESS | DATA | FUNCTION | INITIAL |
|---|---|---|---|---|---|
| 10 (bank 2) | 3 Power-down control | 0011 | XXX0 | analog front-end active | reset |
| | | | XXX1 | analog front-end powered down | – |
| | | | XX0X | buffer amplifier on | reset |
| | | | XX1X | buffer amplifier off (power saving) | – |
| | | | X0XX | DAC active | reset |
| | | | X1XX | DAC powered down | – |
| | 3 DAC output mode | | 0XXX | normal mode | reset |
| | | | 1XXX | current mode (bypass internal I-to-V converters) | – |
| | 7 mechanism and voltage reference selection | 0111 | XX10 | voltage mechanism: $\frac{1.65 \times V_{DDA}}{3.3\ V}$ | reset |
| | | | XX11 | Voltage mechanism: $\frac{2.5 \times V_{DDA}}{3.3\ V}$ | – |
| | | | X0XX | 150 mV mechanism | reset |
| | | | X1XX | 180 mV mechanism | – |
| | 7 CD-text control | | 0XXX | flag all data (CRC pass and fail) | reset |
| | | | 1XXX | flag only data that passes the CRC | – |

| SHADEN BITS | SHADOW REGISTER | ADDRESS | DATA | FUNCTION | INITIAL |
|---|---|---|---|---|---|
| 10 (bank 2) | A laser power control 1 | 1010 | XXX0 | approximately 58% (laser power control 2 = 0) | reset |
| | | | | approximately 72% (laser power control 2 = 1) | |
| | | | | see shadow register 3 (bank 3) | |
| | | | XXX1 | approximately 86% (laser power control 2 = 0) | – |
| | | | | approximately 100% (laser power control 2 = 1) | |
| | | | | see shadow register 3 (bank 3) | |
| | A clock source | | XX0X | bypass PLL (external clock source) | – |
| | | | XX1X | select and enable PLL | reset |
| | A KILL control | | X0XX | disable silence injection | reset |
| | | | X1XX | enable silence injection | – |
| | | | 0XXX | internal KILL | reset |
| | | | 1XXX | loop-back KILL | – |
| | C DC offset measurement times | 1100 | XX00 | settling time = 354 μs | reset |
| | | | XX01 | settling time = 1 ms | – |
| | | | XX10 | settling time = 2 ms | – |
| | | | XX11 | settling time = 10 ms | – |
| | C upsampler dither selection | | 00XX | no dither selected | – |
| | | | 01XX | AC dither only | – |
| | | | 10XX | DC dither only | – |
| | | | 11XX | AC and DC dither selected | reset |

**Table 20** Bank 3 new shadow register settings (single write)

| SHADEN BITS | SHADOW REGISTER | ADDRESS | DATA | FUNCTION | INITIAL |
|---|---|---|---|---|---|
| 11 (bank 3) | 3 diode selection for DC offset measurement | 0011 | X000 | select D1 | reset |
| | | | X001 | select D1 | – |
| | | | X010 | select D2 | – |
| | | | X011 | select D3 | – |
| | | | X100 | select D4 | – |
| | | | X101 | select R1 | – |
| | | | X110 | select R2 | – |
| | | | X111 | select D1 | – |
| | 3 laser power control 2 | | 0XXX | 60% (laser power control 1 = 0) | reset |
| | | | | 87% (laser power control 1 = 1) | |
| | | | | see shadow register A (bank 2) | |
| | | | 1XXX | 73% (laser power control 1 = 0) | – |
| | | | | 100% (laser power control 1 = 1) | |
| | | | | see shadow register A (bank 2) | |
| | C enable equalizer | 1100 | XXX0 | equalizer disabled and powered-down | reset |
| | | | XXX1 | equalizer enabled | – |
| | C STATUS pin control | | 000X | STATUS pin outputs decoder status register information | reset |
| | | | 001X | STATUS pin outputs DC offset ready flag | – |
| | | | 010X | STATUS pin outputs DC offset value | – |

**Table 21** Bank 3 new shadow register settings (multiple write)

| SHADEN BITS | SHADOW REGISTER | ADDRESS | SIZE (DATA NIBBLES) | REGISTER ELEMENTS(1) |
|---|---|---|---|---|
| 11 (bank 3) | 7 DC cancellation levels | 0111 | 9 | <r2_off> <r1_off> <d4_off> <d3_off> <d2_off> <d1_off> |
| | A analog FE control | 1010 | 4 | <hp_filter_sel> <eq_speed_sel> <slicer_slew> <hf_gain> |

**Note**

1. Register elements are described in Tables 26 and 27.

**Table 22** Multiple write register element description

| SHADOW REGISTER | ELEMENT NAME | BIT NUMBERS | DESCRIPTION |
|---|---|---|---|
| 7 (bank 3) | <d1_off> | <5:0> | DC offset level for D1 (reset value = 000000) |
| | <d2_off> | <11:6> | DC offset level for D2 (reset value = 000000) |
| | <d3_off> | <17:12> | DC offset level for D3 (reset value = 000000) |
| | <d4_off> | <23:18> | DC offset level for D4 (reset value = 000000) |
| | <r1_off> | <29:24> | DC offset level for R1 (reset value = 000000) |
| | <r2_off> | <35:30> | DC offset level for R2 (reset value = 000000) |
| A (bank 3) | <hf_gain> | <3:0> | see Table 23 |
| | <slicer_slew> | <7:4> | see Table 24 |
| | <eq_speed_sel> | <9:8> | equaliser operating speed: 00 = 1× (reset); 01 = 2×; 10 = 4× |
| | <hp_filter_sel> | <15:10> | see Table 25 |

**Table 23** HF gain

| DATA | DESCRIPTION |
|---|---|
| 0000 | voltage mode = 1.11 V |
| 0001 | voltage mode = 952 mV |
| 0010 | voltage mode = 588 mV |
| 0011 | voltage mode = 392 mV |
| 0100 | voltage mode = 1.11 V |
| 0101 | voltage mode = 952 mV |
| 0110 | voltage mode = 588 mV |
| 0111 | voltage mode = 392 mV |
| 1000 | voltage mode = 303 mV |
| 1001 | voltage mode = 200 mV |
| 1010 | voltage mode = 157 mV |
| 1011 | voltage mode = 107 mV |
| 1100 | voltage mode = 79 mV |
| 1101 | voltage mode = 54 mV |
| 1110 | voltage mode = 39 mV |
| 1111 | voltage mode = 27 mV |

**Table 24** Slicer threshold tracking slew rate (ISlice code to current conversion)

| DATA | CURRENT (μA) |
|---|---|
| 0000 | 10 (reset) |
| 0001 | 10 |
| 0010 | 20 |
| 0011 | 30 |
| 0100 | 50 |
| 0101 | 60 |
| 0110 | 70 |
| 0111 | 80 |
| 1000 | 100 |
| 1001 | 110 |
| 1010 | 120 |
| 1011 | 130 |
| 1100 | 150 |
| 1101 | 160 |
| 1110 | 170 |
| 1111 | 180 |

**Table 25** High-pass filter frequency cut-off level (lowest roll-off)

| DATA | NOMINAL FREQUENCY (kHz) | PERCENTAGE DEVIATION | ACTUAL FREQUENCY (kHz) |
|---|---|---|---|
| 000000 | 10 | –37.5% | 6.367 (reset) |
| 010000 | | –28.2% | 7.31 |
| 001000 | | –17.6% | 8.395 |
| 011000 | | –9.2% | 9.247 |
| 000100 | | 0% | 10.186 |
| 010100 | | +8.6% | 11.066 |
| 001100 | | +18% | 12.023 |
| 000010 | 20 | –37.5% | 12.706 |
| 010010 | | –28.2% | 14.588 |
| 001010 | | –17.6% | 16.520 |
| 011010 | | –9.2% | 18.45 |
| 000110 | | 0% | 20.324 |
| 010110 | | +8.6% | 22.080 |
| 001110 | | +18% | 23.988 |
| 000001 | 30 | –37.5% | 18.967 |
| 010001 | | –28.2% | 21.777 |
| 001001 | | –17.6% | 24.660 |
| 011001 | | –9.2% | 27.542 |
| 000101 | | 0% | 30.339 |
| 010101 | | +8.6% | 32.961 |
| 001101 | | +18% | 35.318 |
| 000011 | 40 | –37.5% | 25.003 |
| 010011 | | –28.2% | 29.107 |
| 001011 | | –17.6% | 32.961 |
| 011011 | | –9.2% | 36.307 |
| 000111 | | 0% | 39.994 |
| 010111 | | +8.6% | 43.451 |
| 001111 | | +18% | 47.206 |

#### 7.17.6 SUMMARY OF SERVO COMMANDS

A list of the servo commands is given in Table 26. These are fully compatible with the SAA732X.

**Table 26** Servo commands

| COMMANDS | CODE | BYTES | PARAMETERS |
|---|---|---|---|
| **Write commands** | | | |
| Write_focus_coefs1 | 17H | 7 | <foc_parm3> <foc_int> <ramp_incr> <ramp_height> <ramp_offset> <FE_start> <foc_gain> |
| Write_focus_coefs2 | 27H | 7 | <defect_parm> <rad_parm_jump> <vel_parm2> <vel_parm1> <foc_parm1> <foc_parm2> <CA_drop> |
| Write_focus_command | 33H | 3 | <foc_mask> <foc_stat> <FFH> |
| Focus_gain_up | 42H | 2 | <foc_gain> <foc_parm1> |
| Focus_gain_down | 62H | 2 | <foc_gain> <foc_parm1> |
| Write_radial coefs | 57H | 7 | <rad_length_lead> <rad_int> <rad_parm_play> <rad_pole_noise> <rad_gain> <sledge_parm2> <sledge_parm_1> |
| Preset_Latch | 81H | 1 | <chip_init> |
| Radial_off | C1H | 1 | ‘1CH’ |
| Radial_init | C1H | 1 | ‘3CH’ |
| Short_jump | C3H | 3 | <tracks_hi> <tracks_lo> <rad_stat> |
| Long_jump | C5H | 5 | <brake_dist> <sledge_U_max> <tracks_hi> <tracks_lo> <rad_stat> |
| Steer_sledge | B1H | 1 | <sledge_level> |
| Preset_init | 93H | 3 | <re_offset> <re_gain> <sum_gain> |
| Write_decoder_reg(1) | D1H | 1 | <decoder_reg_data> |
| Write_parameter | A2H | 2 | <param_ram_addr> <param_data> |
| **Read commands** | | | |
| Read_Q_subcode(1)(2) | 0H | up to 12 | <Q_sub1 to 10> <peak_l> <peak_r> |
| Read_status | 70H | up to 5 | <foc_stat> <rad_stat> <rad_int_lpf> <tracks_hi> <tracks_lo> |
| Read_hilevel_status(3) | E0H | up to 4 | <intreq> <dec_stat> <seq_stat> <motor_start_time> |
| Read_aux_status | F0H | up to 3 | <re_offset> <re_gain> <sum_gain> |

**Notes**

1. These commands are only available when the decoder interface is enabled.
2. <peak_l> and <peak_r> bytes are clocked out LSB first.
3. Decoder status flag information in, <dec_stat> is only valid when the internal decoder interface is enabled.

#### 7.17.7 SUMMARY OF SERVO COMMAND PARAMETERS

**Table 27** Servo command parameters

| PARAMETER | RAM ADDRESS | AFFECTS | POR VALUE | DETERMINES |
|---|---|---|---|---|
| foc_parm_1 | – | focus PID | – | end of focus lead |
| | | | | defect detector enabling |
| foc_parm_2 | – | focus PID | – | focus low-pass |
| | | | | focus error normalizing |
| foc_parm_3 | – | focus PID | – | focus lead length |
| | | | | minimum light level |
| foc_int | 14H | focus PID | – | focus integrator crossover frequency |
| foc_gain | 15H | focus PID | 70H | focus PID loop gain |
| CA_drop | 12H | focus PID | – | sensitivity of dropout detector |
| ramp_offset | 16H | focus ramp | – | asymmetry of focus ramp |
| ramp_height | 18H | focus ramp | – | peak-to-peak value of ramp voltage |
| ramp_incr | – | focus ramp | – | slope of ramp voltage |
| FE_start | 19H | focus ramp | – | minimum value of focus error |
| rad_parm_play | 28H | radial PID | – | end of radial lead |
| rad_pole_noise | 29H | radial PID | – | radial low-pass |
| rad_length_lead | 1CH | radial PID | – | length of radial lead |
| rad_int | 1EH | radial PID | – | radial integrator crossover frequency |
| rad_gain | 2AH | radial PID | 70H | radial loop gain |
| rad_parm_jump | 27H | radial jump | – | filter during jump |
| vel_parm1 | 1FH | radial jump | – | PI controller crossover frequencies |
| vel_parm2 | 32H | radial jump | – | jump pre-defined profile |
| speed_threshold | 48H | radial jump | – | maximum speed in fastrad mode |
| hold_mult | 49H | radial jump | 00H | electronic damping |
| | | | | sledge bandwidth during jump |
| brake_dist_max | 21H | radial jump | – | maximum sledge distance allowed in fast actuator steered mode |
| sledge_long_brake | 58H | radial jump | FFH | brake distance of sledge |
| sledge_Umax | – | sledge | – | voltage on sledge during long jump |
| sledge_level | – | sledge | – | voltage on sledge when steered |
| sledge_parm_1 | 36H | sledge | – | sledge integrator crossover frequency |
| sledge_parm_2 | 17H | sledge | – | sledge low-pass frequencies |
| | | | | sledge gain |
| | | | | sledge operation mode |
| sledge_pulse1 | 46H | pulsed sledge | – | pulse width |
| sledge_pulse2 | 64H | pulsed sledge | – | pulse height |
| defect_parm | – | defect detector | – | defect detector setting |
| playwatchtime | 54H | Watchdog | – | radial on-track Watchdog time |
| jumpwatchtime | 57H | Watchdog | – | radial jump Watchdog time-out |

| PARAMETER | RAM ADDRESS | AFFECTS | POR VALUE | DETERMINES |
|---|---|---|---|---|
| radcontrol | 59H | Watchdog | – | enable/disable automatic radial off feature |
| chip_init | – | set-up | – | enable/disable decoder interface |
| xtra_preset | 4AH | set-up | 38H | laser on/off |
| | | | | RA, FO and SL PDM modulating frequency |
| | | | | fast jumping circuit on/off |
| cd6cmd | 4DH | decoder interface | – | decoder part commands |
| interrupt_mask | 53H | STATUS pin | – | enabled interrupts |
| seq_control | 42H | autosequencer | – | autosequencer control |
| focus_start_time | 5EH | autosequencer | – | focus start time |
| motor_start_time1 | 5FH | autosequencer | – | motor start 1 time |
| motor_start_time2 | 60H | autosequencer | – | motor start 2 time |
| radial_init_time | 61H | autosequencer | – | radial initialization time |
| brake_time | 62H | autosequencer | – | brake time |
| RadCmdByte | 63H | autosequencer | – | radial command byte |
| osc_inc | 68H | focus/radial AGC | – | AGC control |
| | | | – | frequency of injected signal |
| phase_shift | 67H | focus/radial AGC | – | phase shift of injected signal |
| level1 | 69H | focus/radial AGC | – | amplitude of signal injected |
| level2 | 6AH | focus/radial AGC | – | amplitude of signal injected |
| agc_gain | 6CH | focus/radial AGC | – | focus/radial gain |

## 8 SUMMARY OF SERVO COMMAND PARAMETERS VALUES

**Table 28** foc_parm1 parameter: focus end lead frequency, defect detector, offtrack detector

| **foc_parm1**<br>**foc_pole_lead value (binary)** | **Focus end lead frequency $f_3$ kHz** |
|---|---|
| xxx1 1100 | 1.97 |
| xxx1 1000 | 2.29 |
| xxx0 0000 | 2.61 |
| xxx0 1000 | 2.94 |
| xxx0 1100 | 3.26 |
| xxx1 1101 | 3.90 |
| xxx1 1001 | 4.55 |
| xxx0 0001 | 5.19 |
| xxx0 1001 | 5.82 |
| xxx0 1101 | 6.46 |
| xxx1 1110 | 7.72 |
| xxx1 1010 | 8.98 |
| xxx0 0010 | 10.22 |
| xxx0 1010 | 11.46 |
| xxx0 1110 | 12.69 |
| xxx1 1111 | 15.13 |
| xxx1 1011 | 17.54 |
| xxx0 0011 | 19.93 |
| xxx0 1011 | 22.28 |
| **defect_det_sw** | **Defect detector** |
| x11x xxxx | defect detector does not influence focus and radial |
| x10x xxxx | focus hold on defect detector |
| x00x xxxx | focus and radial hold on defect detector |
| x01x xxxx | undefined, reserved |
| **otd_select** | **Offtrack detector** |
| 0xxx xxxx | ON track active 1 |
| 1xxx xxxx | ON track active 0 |

**Table 29** foc_parm2 parameter: focus low-pass start frequency, focusing system

| **foc_parm2**<br>**foc_pole_noise value (binary)** | **Focus low-pass start frequency $f_4$ kHz** |
|---|---|
| xxx1 1100 | 3.90 |
| xxx1 1000 | 4.55 |
| xxx0 0000 | 5.19 |
| xxx0 1000 | 5.82 |
| xxx0 1100 | 6.46 |
| xxx1 1101 | 7.72 |
| xxx1 1001 | 8.98 |
| xxx0 0001 | 10.22 |
| xxx0 1001 | 11.46 |
| xxx0 1101 | 12.69 |
| xxx1 1110 | 15.13 |
| xxx1 1010 | 17.54 |
| xxx0 0010 | 19.93 |
| xxx0 1010 | 22.28 |
| xxx0 1110 | 25.40 |
| xxx1 1111 | 30.26 |
| xxx1 1011 | 35.08 |
| xxx0 0011 | 39.86 |
| xxx0 1011 | 44.56 |
| **detector_arr** | **Focusing system** |
| xx1x xxxx | single foucault |
| xx0x xxxx | double foucault |

**Table 30** foc_parm3 parameter: focus lead length, CA start level for focus acquisition

| foc_parm3 | Focus lead length $f_3/f_2$ |
|---|---|
| **foc_lead_length value (binary)** | |
| 0000 xxx1 | 64 |
| 1000 xxx1 | 32 |
| 0100 xxx1 | 21.3 |
| 1100 xxx1 | 16 |
| 0010 xxx1 | 12.8 |
| 1010 xxx1 | 10.7 |
| 0110 xxx1 | 9.1 |
| 1110 xxx1 | 8 |
| 0001 xxx1 | 7.1 |
| 1001 xxx1 | 6.4 |
| 0101 xxx1 | 5.8 |
| 1101 xxx1 | 5.3 |
| 0011 xxx1 | 4.9 |
| 1011 xxx1 | 4.6 |
| 0111 xxx1 | 4.3 |
| 1111 xxx1 | 4 |
| **CA_start value (binary)** | **$CA_{min}$** |
| xxxx 000x | 0.0225 |
| xxxx 001x | 0.03 |
| xxxx 010x | 0.045 |
| xxxx 011x | 0.06 |
| xxxx 100x | 0.09 |
| xxxx 101x | 0.125 |
| xxxx 110x | 0.18 |
| xxxx 111x | 1.0 |

**Table 31** CA_drop parameter: CA level for dropout detection

| CA_drop value (binary) | $CA_{min}$ |
|---|---|
| xxx0 0000 | 0.0225 |
| xxx0 0100 | 0.03 |
| xxx0 1000 | 0.045 |
| xxx0 1100 | 0.06 |
| xxx1 0000 | 0.09 |
| xxx1 0100 | 0.125 |
| xxx1 1000 | 0.18 |
| xxx1 1100 | 1.0 |

**Table 32** FE_start parameter: minimum threshold for focus start

| FE_start value (decimal) | Minimum threshold for $(d_1 - d_2)/(d_1 + d_2)$ |
|---|---|
| 0 | always |
| 1 | 1/127 |
| 2 | 2/127 |
| i | i/127 |
| 64 | 64/127 |
| 65...127 | 65 to 127/127 |
| 127 | continuous ramping |
| 128...255 | not allowed |

**Table 33** foc_int_strength parameter: focus integrator strength

| foc_int_strength value (decimal) | Focus integrator strength $f_5$ Hz |
|---|---|
| 0 | integrator hold |
| 1 | 1.2 |
| 2 | 2.4 |
| i | $1.2 \times i$ |
| 21 | 25 |
| 22...255 | undefined |

**Table 34** foc_gain parameter: focus gain

| foc_gain value (decimal) | G |
|---|---|
| 1 | 2048 |
| 2 | 1024 |
| 3 | 2048/3 |
| i | 2048/i |
| 255 | 2048/255 |
| 0 | undefined |

**Table 35** rad_pole_noise parameter: radial low-pass start frequency

| rad_pole_noise value (binary) | Radial low-pass start frequency $f_4$ kHz |
|---|---|
| 1101 1100 | 3.90 |
| 1011 1000 | 4.55 |
| 1010 0000 | 5.19 |
| 1010 1000 | 5.82 |
| 1000 1100 | 6.46 |
| 1001 1101 | 7.72 |
| 1001 1001 | 8.98 |
| 0100 0001 | 10.22 |
| 0100 1001 | 11.46 |
| 0100 1101 | 12.69 |
| 0101 1110 | 15.13 |
| 0101 1010 | 17.54 |
| 0100 0010 | 19.93 |
| 0100 1010 | 22.28 |
| xxx0 1110 | 25.40 |
| xxx1 1111 | 30.26 |
| xxx1 1011 | 35.08 |
| xxx0 0011 | 39.86 |
| xxx0 1011 | 44.56 |

**Table 36** rad_lead_length parameter: radial lead length

| rad_lead_length value (binary) | rad_lead_length value (hex) | Radial lead length $f_3/f_2$ |
|---|---|---|
| 0000 xxxx | 0x | 128 |
| 1000 xxxx | 8x | 64 |
| 0100 xxxx | 4x | 42.7 |
| 1100 xxxx | Cx | 32 |
| 0010 xxxx | 2x | 25.6 |
| 1010 xxxx | Ax | 21.3 |
| 0110 xxxx | 6x | 18.3 |
| 1110 xxxx | Ex | 16 |
| 0001 xxxx | 1x | 14.2 |
| 1001 xxxx | 9x | 12.8 |
| 0101 xxxx | 5x | 11.6 |
| 1101 xxxx | Dx | 10.7 |
| 0011 xxxx | 3x | 9.8 |
| 1011 xxxx | Bx | 9.1 |
| 0111 xxxx | 7x | 8.5 |
| 1111 xxxx | Fx | 8 |

**Table 37** rad_parm_play, rad_parm_jump parameters: radial end lead frequency

| rad_parm_play rad_parm_jump value (binary) | rad_parm_play rad_parm_jump value (hex) | Radial end lead frequency $f_3$ kHz |
|---|---|---|
| 1101 1100 | DC | 1.97 |
| 1101 1000 | D8 | 2.29 |
| 1100 0000 | C0 | 2.61 |
| 1100 1000 | C8 | 2.94 |
| 1100 1100 | CC | 3.26 |
| 1101 1101 | DD | 3.90 |
| 1001 1001 | 99 | 4.55 |
| 1010 0001 | A1 | 5.19 |
| 1010 1001 | A9 | 5.82 |
| 1010 1101 | AD | 6.46 |
| 1001 1110 | 9E | 7.72 |
| 0101 1010 | 5A | 8.98 |
| 0100 0010 | 42 | 10.22 |
| 0100 1010 | 4A | 11.46 |
| 1000 1110 | 8E | 12.69 |
| 0101 1111 | 5F | 15.13 |
| 0101 1011 | 5B | 17.54 |
| 0100 0011 | 43 | 19.93 |
| 0100 1011 | 4B | 22.28 |

**Table 38** rad_gain parameter: radial PID gain

| rad_gain value (decimal) | Radial PID gain G |
|---|---|
| 1 | 256 |
| 2 | 256/2 |
| 3 | 256/3 |
| i | 256/i |
| 255 | 256/255 |
| 0 | undefined |

**Table 39** rad_int_strength parameter: radial integrator strength

| rad_int_strength value (decimal) | Radial integrator strength $f_5$ Hz |
|---|---|
| 0 | integrator hold |
| 1 | 0.3 |
| 2 | 0.6 |
| i | $0.31 \times i$ |
| 255 | 79.05 |

**Table 40** Sledge_parm1 parameter: sledge integrator bandwidth, shock filter (low-pass, high-pass selection); RAM address 36H

| sledge_parm1 | Sledge integrator $f_1$ Hz |
|---|---|
| sledge_int | |
| x00x xxxx | integrator disabled |
| x10x xxxx | 0.15 |
| x01x xxxx | 0.31 |
| x11x xxxx | 0.45 |

**Table 41** sledge_parm2 parameter: sledge gain, low-pass frequencies, operation mode; RAM address 17H

| sledge_parm2 / sledge_gain | Sledge gain $G_S$ |
|---|---|
| 0xxx x000 | 0.218 |
| 0xxx x001 | 0.281 |
| 0xxx x010 | 0.436 |
| 0xxx x011 | 0.562 |
| 0xxx x100 | 0.875 |
| 0xxx x101 | 1.125 |
| 0xxx x110 | 1.750 |
| 0xxx x111 | 2.250 |
| 1xxx x000 | 3.500 |
| 1xxx x001 | 4.500 |
| 1xxx x010 | 7.000 |
| 1xxx x011 | 9.000 |
| 1xxx x100 | 14.00 |
| 1xxx x101 | 18.00 |
| 1xxx x110 | 28.00 |
| 1xxx x111 | 36.00 |
| **sledge_low_pass** | **Sledge low-pass frequency $f_2$ Hz** |
| x00x 0xxx | 5.0 |
| x10x 0xxx | 10.1 |
| x01x 0xxx | 15.3 |
| x11x 0xxx | 20.5 |
| x00x 1xxx | 0.3 |
| x10x 1xxx | 0.6 |
| x01x 1xxx | 0.9 |
| x11x 1xxx | 1.2 |
| **sledge_op_mode** | **Sledge operation mode** |
| xxx0 0xxx | PI mode operation |
| xxx0 1xxx | pulsed mode operation, microcontroller controlled |
| xxx1 1xxx | pulsed mode operation, automatic mode |

**Table 42** sledge_pulse1 parameter: sledge pulse high time, low time; RAM address 46H

| sledge_pulse1 / time_lo | Hex | Time low ms |
|---|---|---|
| 0000 xxxx | 0x | 0 |
| 0001 xxxx | 1x | 2 |
| 0010 xxxx | 2x | 4 |
| 0011 xxxx | 3x | 6 |
| 0100 xxxx | 4x | 8 |
| 0101 xxxx | 5x | 10 |
| 0110 xxxx | 6x | 12 |
| 0111 xxxx | 7x | 14 |
| 1000 xxxx | 8x | 16 |
| 1001 xxxx | 9x | 18 |
| 1010 xxxx | Ax | 20 |
| 1011 xxxx | Bx | 22 |
| 1100 xxxx | Cx | 24 |
| 1101 xxxx | Dx | 26 |
| 1110 xxxx | Ex | 28 |
| 1111 xxxx | Fx | 30 |
| **time_hi** | | **Time high ms** |
| xxxx 0000 | x0 | 0 |
| xxxx 0001 | x1 | 2 |
| xxxx 0010 | x2 | 4 |
| xxxx 0011 | x3 | 6 |
| xxxx 0100 | x4 | 8 |
| xxxx 0101 | x5 | 10 |
| xxxx 0110 | x6 | 12 |
| xxxx 0111 | x7 | 14 |
| xxxx 1000 | x8 | 16 |
| xxxx 1001 | x9 | 18 |
| xxxx 1010 | xA | 20 |
| xxxx 1011 | xB | 22 |
| xxxx 1100 | xC | 24 |
| xxxx 1101 | xD | 26 |
| xxxx 1110 | xE | 28 |
| xxxx 1111 | xF | 30 |

**Table 43** sledge_pulse2 parameter: sledge pulse height; RAM address 64H

| sledge_pulse2 | Hex | Pulse height |
|---|---|---|
| 0111 1111 | 78 | full-scale, positive |
| .... | .... | |
| 0100 0000 | 40 | half-scale, positive |
| a | | level = a/7F, positive |
| 0000 0000 | 00 | zero |
| .... | .... | |
| 1000 0000 | 80 | full-scale, negative |

**Table 44** vel_parm1 parameter: gain constant for short jump, integrator cross-over frequency during jump; RAM address 1FH

| vel_parm1<br>vel_prop | Hex | Gain constant for short jump $K_v$ |
|---|---|---|
| 0000 xxxx | 0x | 0.1875 |
| 1000 xxxx | 8x | 0.4375 |
| 0100 xxxx | 4x | 0.6875 |
| 1100 xxxx | Cx | 0.9375 |
| 0010 xxxx | 2x | 1.1875 |
| 1010 xxxx | Ax | 1.4375 |
| 0110 xxxx | 6x | 1.6875 |
| 1110 xxxx | Ex | 1.9375 |
| 0001 xxxx | 1x | 2.1875 |
| 1001 xxxx | 9x | 2.4375 |
| 0101 xxxx | 5x | 2.6875 |
| 1101 xxxx | Dx | 2.9375 |
| 0011 xxxx | 3x | 3.1875 |
| 1011 xxxx | Bx | 3.4375 |
| 0111 xxxx | 7x | 3.6875 |
| 1111 xxxx | Fx | 3.9375 |
| **vel_int** | | **Integrator cross-over frequency during jump $f_0$** |
| xxxx 0000 | x0 | integrator hold |
| xxxx 0001 | x1 | $10.0/K_v$ |
| xxxx 0010 | x2 | $20.0/K_v$ |
| xxxx 0011 | x3 | $30.0/K_v$ |
| i | | $i \times 10.0/K_v$ |
| xxxx 1111 | xF | $150.0/K_v$ |

**Table 45** vel_parm2 parameter: time constant during sledge access/actuator access, minimum jump speed during short jump; RAM address 32H

| vel_parm2<br>vel_setp (binary) | Hex | Deceleration time fast actuator steered ms | Deceleration time sledge steered ms |
|---|---|---|---|
| 0000 xxxx | 0x | 7.5 | 7.5 |
| 1000 xxxx | 8x | 8.2 | 8.2 |
| 0100 xxxx | 4x | 9 | 9 |
| 1100 xxxx | Cx | 9.7 | 9.7 |
| 0010 xxxx | 2x | 10.5 | 10.5 |
| 1010 xxxx | Ax | 11.2 | 11.2 |
| 0110 xxxx | 6x | 12.5 | 12.5 |
| 1110 xxxx | Ex | 14 | 14 |
| 0001 xxxx | 1x | 15.5 | 15.5 |
| 1001 xxxx | 9x | 16.5 | 16.5 |
| 0101 xxxx | 5x | 20.7 | 20.7 |
| 1101 xxxx | Dx | 25 | 25 |
| 0011 xxxx | 3x | 31.2 | 31.2 |
| 1011 xxxx | Bx | 41 | 41 |
| 0111 xxxx | 7x | 63 | 63 |
| 1111 xxxx | Fx | 128 | 128 |
| **vel_min** | | **$V_1$ minimum jump speed kHz** | |
| xxxx 0000 | x0 | 0.0 | |
| xxxx 0001 | x1 | 1.0 | |
| xxxx 0010 | x2 | 2.0 | |
| xxxx 0011 | x3 | 3.0 | |
| xxxx 0100 | x4 | 4.0 | |
| xxxx 0101 | x5 | 5.0 | |
| xxxx 0110 | x6 | 6.0 | |
| xxxx 0111 | x7 | 7.0 | |
| xxxx 1xxx | | undefined | |

**Table 46** brake_dist_max parameter: maximum sledge distance allowed in fast actuator steered mode; RAM address 21H

| brake_dist_max value (decimal) | Maximum sledge distance allowed in fast actuator steered mode, number of tracks |
|---|---|
| 0...127 | not allowed |
| –1 | $1 \times 16$ |
| –2 | $2 \times 16$ |
| .... | .... |
| –i | $i \times 16$ |
| .... | .... |
| –127 | $127 \times 16$ |
| –128 | $128 \times 16$ |

**Table 47** sledge_Umax parameter: voltage on sledge during long jump

| sledge_Umax (decimal) | voltage on sledge |
|---|---|
| 127 | $255/256 \times V_{DD}$ |
| i | $(i + 128)/256 \times V_{DD}$ |
| 0 | $0.5 \times V_{DD}$ |
| –1 | $(128 - 1)/256 \times V_{DD}$ |
| –i | $(-i + 128)/256 \times V_{DD}$ |
| –128 | 0 |

**Table 48** sledge_level parameter: voltage on sledge when steered

| sledge_level (decimal) | voltage on sledge |
|---|---|
| 127 | $127/256 \times V_{DD}$ |
| i | $i/256 \times V_{DD}$ |
| 0 | 0 |
| –1 | $-1/256 \times V_{DD}$ |
| –i | $-i/256 \times V_{DD}$ |
| –128 | $-128/256 \times V_{DD}$ |

**Table 49** jumpwatchtime parameter: radial jump watchdog readout time difference; RAM address 57H

| jumpwatchtime | Radial jump watchdog readout time difference ms |
|---|---|
| 80H to FFH | none |
| 0H | 0 |
| 1H | 0.25 |
| i | $i \times 0.25$ |
| 7FH | 32 |

**Table 50** playwatchtime parameter: radial play watchdog maximum time-out; RAM address 54H

| playwatchtime | Radial play watchdog maximum time-out ms |
|---|---|
| 80H | 0 |
| 81H | 0.5 |
| 82H | 1 |
| i | $(i - 80H) \times 0.5$ |
| 00H | 64 |
| j | $(j + 80H) \times 0.5$ |
| 7fH | 128 |

**Table 51** radcontrol parameter: automatic radial servo switch-off control; RAM address 59H

| radcontrol | Hex | Automatic radial servo switch-off control |
|---|---|---|
| 0000 0000 | 00 | radial servo not influenced by watchdog |
| 0100 0000 | 40 | switch-off radial servo on jump error; no action on play error |
| 0010 0000 | 20 | switch-off radial servo on play error; no action on jump error |
| 0110 0000 | 60 | switch-off radial servo on play or jump error |

**Table 52** hold_mult parameter: velocity proportional part during long jump, sledge gain in steered sledge mode; RAM address 49H

| hold_mult<br>vel_prop1 (binary) | Hex | Velocity proportional part during long jump $K_p$ |
|---|---|---|
| 0000 xxxx | 0x | 0 |
| 1000 xxxx | 8x | 0.015625 |
| 0100 xxxx | 4x | 0.031250 |
| 1100 xxxx | Cx | 0.046875 |
| 0010 xxxx | 2x | 0.062500 |
| 1010 xxxx | Ax | 0.078125 |
| 0110 xxxx | 6x | 0.093750 |
| 1110 xxxx | Ex | 0.109375 |
| 0001 xxxx | 1x | 0.125000 |
| 1001 xxxx | 9x | 0.140625 |
| 0101 xxxx | 5x | 0.156250 |
| 1101 xxxx | Dx | 0.171875 |
| 0011 xxxx | 3x | 0.187500 |
| 1011 xxxx | Bx | 0.203125 |
| 0111 xxxx | 7x | 0.218750 |
| 1111 xxxx | Fx | 0.234375 |
| **vel_prop2** | | **Sledge gain in steered mode $G_S$** |
| xxxx x000 | x0 | 2 |
| xxxx x001 | x1 | 3 |
| xxxx x010 | x2 | 4 |
| xxxx x011 | x3 | 6 |
| xxxx x100 | x4 | 8 |
| xxxx x101 | x5 | 12 |
| xxxx x110 | x6 | 16 |
| xxxx x111 | x7 | 24 |

**Table 53** speed_threshold parameter: maximum sledge speed allowed in fast actuator steered mode; RAM address 48H

| speed_threshold value (decimal) | Maximum sledge speed allowed in fast actuator steered mode, number of tracks (x 1000 tracks/sec) |
|---|---|
| 0...127 | not allowed |
| –1 | 1 |
| –2 | 2 |
| –3...–127 | 3...127 |
| –128 | 128 |
| –64 | reset value |

**Table 54** sledge_long_brake parameter: maximum sledge distance allowed in sledge steered mode; RAM address 58H

| sledge_long_brake (decimal) | Maximum sledge distance allowed in sledge steered mode, number of tracks |
|---|---|
| –1...–128 | test always true |
| 1 | 1 × 128 |
| 2 | 2 × 128 |
| 3...62 | 3 × 128...62 × 128 |
| 63 | 63 × 128 |
| –1 | reset value |

**Table 55** defect_parm parameter: defect detector control

| defect_parm | Fast filter bandwidth | |
|---|---|---|
| xxxx xx00 | 3500 Hz | |
| xxxx xx01 | 7000 Hz | |
| xxxx xx10 | 14000 Hz | |
| xxxx xx11 | reserved for future use | |
| **defect_parm** | **Slow filter time constant** | **Alpha value** |
| xxxx 10xx | 16 ms | 0.00006 |
| xxxx 11xx | 8 ms | 0.00012 |
| xxxx 00xx | 4 ms | 0.00024 |
| xxxx 01xx | 2 ms | 0.00048 |
| **defect_parm** | **Coefficient β value** | |
| xx00 xxxx | 0.25 | |
| xx01 xxxx | 0.125 | |
| xx10 xxxx | 0.0625 | |
| xx11 xxxx | reserved for future use | |
| **defect_parm** | **Defect detector maximum ON time** | |
| 00xx xxxx | 1.0 ms | |
| 01xx xxxx | 1.5 ms | |
| 10xx xxxx | 2.0 ms | |
| 11xx xxxx | 2.5 ms | |

**Table 56** interrupt_mask parameter: mask to enable interrupt in interrupt status register; RAM address 53H

| interrupt_mask | Interrupt enabled |
|---|---|
| 0000 0000 | no interrupt |
| xxxx xxx1 | focus lost |
| xxxx xx1x | subcode ready |
| xxxx x1xx | subcode absolute seconds changed |
| xxxx 1xxx | subcode discontinuity |
| xxx1 xxxx | radial error |
| xx1x xxxx | autosequencer state changes |
| x1xx xxxx | autosequencer error |

**Table 57** time_parameter: timer interrupt values

| time_parameter value (decimal)(1) | Timer interrupt values wait time (ms) |
|---|---|
| $129 \le i \le 143$ | $4.26 \times (i - 128)$ |
| $144 \le i \le 159$ | $68.2 + 4.57 \times (i - 144)$ |
| $160 \le i \le 175$ | $141.4 + 4.92 \times (i - 160)$ |
| $176 \le i \le 191$ | $224.1 + 5.33 \times (i - 176$ |
| $192 \le i \le 207$ | $305.4 + 5.82 \times (i - 192$ |
| $208 \le i \le 223$ | $398.5 + 6.40 \times (i - 208)$ |
| $224 \le i \le 239$ | $500.8 + 7.11 \times (i - 224$ |
| $2402 \le i \le 55$ | $614.6 + 8.00 \times (i - 240)$ |
| $0 \le i \le 15$ | $742.6 + 9.11 \times i$ |
| $16 \le i \le 31$ | $888.9 + 10.6 \times (i - 16)$ |
| $32 \le i \le 47$ | $1059 + 12.8 \times (i - 32)$ |
| $48 \le i \le 63$ | $1263 + 16.0 \times (i - 48)$ |
| $64 \le i \le 79$ | $1519 + 21.2 \times (i - 64)$ |
| $80 \le i \le 95$ | $1860 + 32.0 \times (i - 80)$ |
| $96 \le i \le 111$ | $2372 + 64.0 \times (i - 96)$ |
| 111 | 3398.0 |
| 112...127 | infinite |

**Note**

1. The time_parameter values are also used for focus_start_time, motor_start_time1, motor_start_time2, radial_init_time and brake_time.

**Table 58** phase_shift parameter: focus/radial AGC detection phase shift; RAM address 67H

| phase_shift (decimal) | Focus/radial AGC detection phase shift | |
|---|---|---|
| | (μs) | (deg) |
| 0 | 0 | 0 |
| $1 \times a$(1) | 60.47 | $180 \times (a/128)$ |
| $2 \times a$ | 120.94 | $180 \times (2 \times a/128)$ |
| $i \times a$ | $i \times 60.47$ | $180 \times (i \times a/128)$ |
| 128 | | 180 |
| $-1 \times a$ | −60.47 | $-180 \times (a/128)$ |
| $-2 \times a$ | −120.94 | $-180 \times (2 \times a/128)$ |
| $-i \times a$ | $-i \times 60.47$ | $-180 \times (i \times a/128)$ |
| 128 | | 180 |

**Note**

1. The value a is the value programmed in Table 60 as the 6 LSBs of osc_inc.

**Table 59** level1, level2 parameter: amplitude of signal injected into focus/radial AGC; RAM address level1 = 69H, level2 = 6AH

| level1, level2 (decimal) | Amplitude of injected signal |
|---|---|
| 0 | 0 |
| 1 to 126 | higher |
| 127 | highest |
| 128 to 255 | not allowed |

**Table 60** osc_inc parameter: focus/radial AGC system control, oscillator frequency; RAM address 68H

| osc_inc | Oscillator frequency Hz |
|---|---|
| xx00 0000 | 0 |
| xx00 0001 | 64.6 |
| xx00 0010 | 129.2 |
| xx00 0011 | 193.8 |
| a | a × 64.6 |
| xx11 1111 | 4069.8 |
| | **AGC control** |
| 00xx xxxx | AGC system off |
| 11xx xxxx | focus AGC active |
| 01xx xxxx | radial AGC active |

**Table 61** re_offset parameter: initial value setting

| re_offset | Value |
|---|---|
| 127 | 128/256 |
| i | i/256 |
| 0 | 0 |
| –i | –i/256 |
| –128 | –128/256 |

**Table 62** re_gain parameter: initial value setting

| re_gain | Value |
|---|---|
| –128 | not allowed |
| –127 | 1/256 |
| –i | (–i + 128)/256 |
| –1 | 127/256 |
| 0 | 128/256 |
| 1 | 129/256 |
| i | (i + 128)/256 |
| 127 | 255/256 |

**Table 63** sum_gain parameter: initial value setting

| sum_gain | Value |
|---|---|
| –128 | not allowed |
| –127 | 1/256 |
| –i | (–i + 128)/256 |
| –1 | 127/256 |
| 0 | 128/256 |
| 1 | 129/256 |
| i | (i + 128)/256 |
| 127 | 255/256 |

## 9 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|---|---|---|---|---|---|
| $V_{DDD}$ | digital supply voltage | internal rail | –0.5 | +2.5 | V |
| | | external rail | –0.5 | +4.6 | V |
| $V_{I(max)}$ | maximum input voltage | | | | |
| | any input | notes 1, 2 and 3 | –0.5 | $V_{DDD}$ + 0.5 | V |
| | 5 V tolerant pins | | –0.5 | +6.0 | V |
| $V_O$ | any output voltage | | –0.5 | $V_{DDD}$ | V |
| $I_{DDD}$ | digital supply current per supply pin | note 4 | – | 20 | mA |
| $I_{SSD}$ | digital ground current per supply pin | note 4 | – | 20 | mA |
| $V_{es}$ | electrostatic handling voltage | note 5 | –2000 | +2000 | V |
| | | note 6 | –200 | +200 | V |
| $T_{amb}$ | ambient temperature | | 0 | 70 | °C |
| $T_{stg}$ | storage temperature | | –55 | +125 | °C |

**Notes**

1. Must not exceed 4.2 V.
2. Including voltage on outputs in 3-state mode.
3. Only valid when both supply voltages are present.
4. The peak current is limited to 25 times the corresponding maximum current.
5. Human body model.
6. Machine model.

## 10 CHARACTERISTICS

$V_{DDD}$ = 1.65 to 1.95 V; $V_{DDA}$ = 3.0 to 3.6 V; $V_{SS}$ = 0 V; $T_{amb}$ = 0 to 70 °C; unless otherwise specified.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| **Supplies** | | | | | | |
| $V_{DDD}$ | digital supply voltage | | 1.65 | 1.8 | 1.95 | V |
| $I_{DDD}$ | digital supply current | n = 1 mode | – | 4.0 | – | mA |
| | | n = 2 mode | – | 5.0 | – | mA |
| | | n = 4 mode | – | 6.0 | – | mA |
| $V_{DDA}$ | analog supply voltage | | 3.0 | 3.3 | 3.6 | V |
| $I_{DDA}$ | analog supply current | n = 1 mode | – | 34 | – | mA |
| | | n = 2 mode | – | 34 | – | mA |
| | | n = 4 mode | – | 34 | – | mA |
| **DEM DAC output ($V_{pos}$ = 3.3 V, $V_{SS}$ = 0 V, $V_{neg}$ = 0 V and $T_{amb}$ = 25 °C)** | | | | | | |
| DIFFERENTIAL OUTPUTS: PINS DACLN, DACLP, DACRN AND DACRP | | | | | | |
| S/N | signal-to-noise ratio | note 1 | – | 90 | – | dB |
| (THD + N)/S | total harmonic distortion plus noise-to-signal ratio | note 2 | – | – | –80 | dB |
| **Headphone buffer ($V_{pos}$ = 3.3 V, $V_{SS}$ = 0 V, $V_{neg}$ = 0 V and $T_{amb}$ = 25 °C)** | | | | | | |
| OUTPUTS: PINS BUFOUTR AND BUFOUTL | | | | | | |
| S/N | signal-to-noise ratio | | – | 85 | – | dB |
| (THD + N)/S | total harmonic distortion plus noise-to-signal ratio | note 3 | – | – | –80 | dB |
| INPUTS: PINS BUFINR AND BUFINL | | | | | | |
| $Z_i$ | input impedance | | – | 47 | – | kΩ |
| **Servo and decoder analog functions ($V_{DDA}$ = 3.3 V, $V_{SSA}$ = 0 V and $T_{amb}$ = 25 °C)** | | | | | | |
| REFERENCE GENERATOR: PIN $I_{REF}$ | | | | | | |
| $V_{IREF}$ | reference voltage level | | 1.16 | 1.26 | 1.36 | V |
| $I_{REF}$ | input reference current | | – | 50 | – | μA |
| $R_{IREF(ext)}$ | external resistance | | – | 24 | – | kΩ |
| DIODE VOLTAGE INPUT: PINS D1 TO D4, R1 AND R2 | | | | | | |
| $V_{i(D)(max)}$ | maximum input voltage for central diode input signal | voltage mode | 0 | – | 960 | mV |
| $V_{i(R)(max)}$ | maximum input voltage for satellite diode input signal | voltage mode | 0 | – | 960 | mV |
| $V_{ref(int)}$ | internally generated reference voltage | $V_{ref\_sel}$ = 10 | – | note 4 | – | V |
| | | $V_{ref\_sel}$ = 11 | – | note 5 | – | V |
| $B_{HF}$ | high frequency bandwidth (D1 to D4) | at 0 dB | 5 | – | – | MHz |
| $G_{tol(HF)}$ | high frequency gain tolerance | | –20 | – | +20 | % |

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $B_{LF}$ | low frequency bandwidth (D1 to D4, R1 and R2) | at 0 dB | 20 | – | – | kHz |
| $(THD + N)/S_{LF}$ | low frequency total harmonic distortion plus noise-to-signal ratio | at 0 dB | – | –50 | –40 | dB |
| $S/N_{LF}$ | low frequency signal-to-noise ratio | | 55 | – | – | dB |
| $G_{tol(LF)}$ | low frequency gain tolerance | | –20 | – | +20 | % |
| $\Delta G_{v(LF)}$ | low frequency variation of gain between channels | | –3 | – | +3 | % |
| $\alpha_{cs(LF)}$ | low frequency channel separation | | – | 60 | – | dB |
| **Laser drive circuit ($V_{DDA}$ = 3.3 V; $V_{SSA}$ = 0 V; $T_{amb}$ = 25 °C; $R_{IREF}$ = 30 kΩ)** | | | | | | |
| $I_{o(LASER)}$ | output current | $V_{LASER}$ = 1 V – ($V_{DDA}$ – 0.6 V) | 10 | 50 | 120 | mA |
| SNR | signal-to-noise ratio | $I_o$ = 50 mA; B = 20 MHz | – | 40 | – | dB |
| $I_{LFPOWER(max)}$ | maximum laser supply current | $I_o$ = 120 mA | – | – | 140 | mA |
| $V_{MONITOR1}$ | monitor diode voltage 1 | maximum power; sel180 = 0 | 140 | 150 | 160 | mV |
| $V_{MONITOR2}$ | monitor diode voltage 2 | maximum power; sel180 = 1 | 170 | 180 | 190 | mV |
| $R_i$ | input resistance | | 10 | – | – | MΩ |
| $V_{sense}$ | sense voltage | | –100 | – | +100 | mV |
| $P_{step}$ | laser output power range | | 43 | – | 100 | % |
| $I_{pd}$ | power-down supply current | | – | – | 10 | µA |
| $I_{LASER(off)}$ | laser off current | | – | – | 30 | mA |
| **Digital inputs** | | | | | | |
| PIN $\overline{RESET}$ (5 V TOLERANT; TTL INPUTS WITH PULL-UP RESISTOR AND HYSTERESIS) | | | | | | |
| $V_{IH}$ | HIGH-level input voltage | | 2.0 | – | – | V |
| $V_{IL}$ | LOW-level input voltage | | – | – | 0.8 | V |
| $V_{hys}$ | hysteresis voltage | | 0.3 | – | – | V |
| $I_{PU}$ | pull-up current | $V_i$ = 0 to $V_{DDD}$; notes 6 and 7 | –31 | – | –68 | µA |
| $t_{W(L)}$ | pulse width (active LOW) | $\overline{RESET}$ only | 1 | – | – | µs |
| PINS V1 AND V2 (CMOS INPUTS) | | | | | | |
| $V_{IH}$ | HIGH-level input voltage | | 2.0 | – | – | V |
| $V_{IL}$ | LOW-level input voltage | | – | – | 0.8 | V |

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| PINS TEST1 TO TEST4 (5 V TOLERANT; TTL INPUTS WITH PULL-DOWN RESISTORS) | | | | | | |
| $V_{IH}$ | HIGH-level input voltage | | 2.0 | – | – | V |
| $V_{IL}$ | LOW-level input voltage | | – | – | 0.8 | V |
| $I_{PD}$ | pull-down current | $V_i$ = 0 to $V_{DDD}$; notes 6 and 7 ($V_i$ = 5 V; note 8) | 20 | 50 | 75 | μA |
| PINS RCK, WCLI, SDI AND SCLI (5 V TOLERANT; TTL INPUTS) | | | | | | |
| $V_{IH}$ | HIGH-level input voltage | | 2.0 | – | – | V |
| $V_{IL}$ | LOW-level input voltage | | – | – | 0.8 | V |
| $I_{IL}$ | LOW-level input current | $V_i$ = 0; no pull-up | – | – | 1 | μA |
| $I_{IH}$ | HIGH-level input current | $V_i$ = $V_{DDD}$; no pull-down | – | – | 1 | μA |
| PINS SCL, SILD, RAB AND CDTCLK (5 V TOLERANT TTL INPUTS WITH HYSTERESIS) | | | | | | |
| $V_{IH}$ | HIGH-level input voltage | | 2.0 | – | – | V |
| $V_{IL}$ | LOW-level input voltage | | – | – | 0.8 | V |
| $I_{IL}$ | LOW-level input current | $V_i$ = 0; no pull-up | – | – | 1 | μA |
| $I_{IH}$ | HIGH-level input current | $V_i$ = $V_{DDE}$; no pull-down | – | – | 1 | μA |
| $V_{hys}$ | hysteresis voltage | | 0.3 | – | – | V |
| **3-state outputs** | | | | | | |
| PINS SCLK, WCLK, DATA, CLK16, RA, FO, SL, SBSY, SFSY, CLK4/12, STATUS, MOTO1 AND MOTO2 (5 V TOLERANT CMOS OUTPUTS; 10 ns SLEW RATE LIMITED) | | | | | | |
| $V_{OL}$ | LOW-level output voltage | $I_{OL}$ = 4 mA | – | – | 0.4 | V |
| $V_{OH}$ | HIGH-level output voltage | $I_{OH}$ = –4 mA | $V_{DDD}$ – 0.4 | – | – | V |
| $I_{OL}$ | LOW-level output current | $V_{OL}$ = 0.4 V; note 9 | 4 | – | – | mA |
| $I_{OH}$ | HIGH-level output current | $V_{OL}$ = $V_{DDD}$ – 0.4 V; note 9 | –4 | – | – | mA |
| $t_{tran(L-H)}$ | LOW-to-HIGH transition time | $C_L$ = 30 pF | 10.2 | – | 14.5 | ns |
| $I_{OZ}$ | 3-state leakage current | $V_i$ = 0; no pull-up or pull-down | – | – | 1 | μA |
| PINS DOBM, V4 AND V5 (5 V TOLERANT CMOS OUTPUTS; 5 ns SLEW RATE LIMITED) | | | | | | |
| $V_{OL}$ | LOW-level output voltage | $I_{OL}$ = 4 mA | – | – | 0.4 | V |
| $V_{OH}$ | HIGH-level output voltage | $I_{OH}$ = –4 mA | $V_{DDD}$ – 0.4 | – | – | V |
| $I_{OL}$ | LOW-level output current | $V_{OL}$ = 0.4 V; note 9 | 4 | – | – | mA |
| $I_{OH}$ | HIGH-level output current | $V_{OL}$ = $V_{DDD}$ – 0.4 V; note 9 | –4 | – | – | mA |
| $t_{tran(L-H)}$ | LOW-to-HIGH transition time | $C_L$ = 30 pF | – | 10 | 13.8 | ns |
| $I_{OZ}$ | 3-state leakage current | $V_i$ = 0; no pull-up or pull-down | – | – | 1 | μA |

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| **Digital inputs and outputs** | | | | | | |
| PIN V3 (5 V TOLERANT; TTL INPUT; 3-STATE OUTPUT) | | | | | | |
| $V_{IH}$ | HIGH-level input voltage | | 2.0 | – | – | V |
| $V_{IL}$ | LOW-level input voltage | | – | – | 0.8 | V |
| $I_{IL}$ | LOW-level input current | $V_i = 0$; no pull-up | – | – | 1 | µA |
| $I_{IH}$ | HIGH-level input current | $V_i = V_{DDD}$; no pull-down | – | – | 1 | µA |
| $V_{OL}$ | LOW-level output voltage | $I_{OL} = 4$ mA | – | – | 0.4 | V |
| $V_{OH}$ | HIGH-level output voltage | $I_{OH} = –4$ mA | $V_{DDD} – 0.4$ | – | – | V |
| $I_{OL}$ | LOW-level output current | $V_{OL} = 0.4$ V; note 9 | 4 | – | – | mA |
| $I_{OH}$ | HIGH-level output current | $V_{OL} = V_{DDD} – 0.4$ V; note 9 | –4 | – | – | mA |
| $t_{tran(L-H)}$ | LOW-to-HIGH transition time | $C_L = 30$ pF | 2.6 | – | 6.3 | ns |
| $I_{OZ}$ | 3-state leakage current | $V_i = 0$ | – | – | 1 | µA |
| PINS LKILL, RKILL AND CFLAG (5 V TOLERANT; TTL INPUT WITH PULL-UP; 3-STATE OPEN-DRAIN OUTPUT; 10 ns SLEW RATE LIMITED) | | | | | | |
| $V_{IH}$ | HIGH-level input voltage | | 2.0 | – | – | V |
| $V_{IL}$ | LOW-level input voltage | | – | – | 0.8 | V |
| $I_{PU}$ | pull-up current | $V_i = 0$ to $V_{DDD}$; notes 6 and 7 | –13 | – | –36 | µA |
| $V_{OL}$ | LOW-level output voltage | $I_{OL} = 4$ mA | – | – | 0.4 | V |
| $V_{OH}$ | HIGH-level output voltage | $I_{OH} = –4$ mA | $V_{DDD} – 0.4$ | – | – | V |
| $I_{OL}$ | LOW-level output current | $V_{OL} = 0.4$ V; note 9 | 4 | – | – | mA |
| $I_{OH}$ | HIGH-level output current | $V_{OL} = V_{DDD} – 0.4$ V; note 9 | –4 | – | – | mA |
| $t_{tran(L-H)}$ | LOW-to-HIGH transition time | $C_L = 30$ pF | 8.6 | 10 | 13.8 | ns |
| $I_{OZ}$ | 3-state leakage current | $V_i = 0$ | – | – | 1 | µA |
| PINS CDTRDY, CDTDATA, EF AND SUB (5 V TOLERANT; TTL INPUT; 3-STATE OUTPUT; 10 ns SLEW RATE LIMITED) | | | | | | |
| $V_{IH}$ | HIGH-level input voltage | | 2.0 | – | – | V |
| $V_{IL}$ | LOW-level input voltage | | – | – | 0.8 | V |
| $I_{IL}$ | LOW-level input current | $V_i = 0$ | – | – | 1 | µA |
| $I_{IH}$ | HIGH-level input current | $V_i = V_{DDD}$ | – | – | 1 | µA |
| $V_{OL}$ | LOW-level output voltage | $I_{OL} = 4$ mA | – | – | 0.4 | V |
| $V_{OH}$ | HIGH-level output voltage | $I_{OH} = –4$ mA | $V_{DDD} – 0.4$ | – | – | V |
| $I_{OL}$ | LOW-level output current | $V_{OL} = 0.4$ V; note 9 | 4 | – | – | mA |
| $I_{OH}$ | HIGH-level output current | $V_{OL} = V_{DDD} – 0.4$ V; note 9 | –4 | – | – | mA |
| $t_{tran(L-H)}$ | LOW-to-HIGH transition time | $C_L = 30$ pF | 8.6 | 10 | 13.8 | ns |
| $I_{OZ}$ | 3-state leakage current | $V_i = 0$ | – | – | 1 | µA |

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| PIN SDA (5 V TOLERANT; 400 kHz I²C-BUS PAD) | | | | | | |
| $V_{IH}$ | HIGH-level input voltage | | $0.7V_{TOL}$ | – | – | V |
| $V_{IL}$ | LOW-level input voltage | $V_{TOL}$ = 5 V; note 10 | – | – | $0.3V_{TOL}$ | V |
| $V_{hys}$ | hysteresis voltage | | $0.05V_{TOL}$ | – | – | V |
| $V_{OL}$ | LOW-level output voltage | $I_{OL}$ = 3 mA | – | – | 0.4 | V |
| $t_f$ | output fall time from $V_{IH}$ to $V_{IL}$ | bus capacitance, $C_b$, from 10 pF to 400 pF) | 20 + $0.1C_b$ | – | 250 | ns |
| $I_{ikg}$ | steady-state current input signal | $V_i$ = $V_{DDD}$; note 11 | – | 2 | 4 | μA |
| | | $V_i$ = 5 V; note 11 | – | 10 | 22 | μA |
| **Crystal oscillator** | | | | | | |
| INPUT: PIN OSCIN (EXTERNAL CLOCK) | | | | | | |
| $V_{IH}$ | HIGH-level input voltage | | – | – | $0.2V_{DDD}$ | V |
| $V_{IL}$ | LOW-level input voltage | | $0.8V_{DDD}$ | – | – | V |
| OUTPUT: PIN OSCOUT; see Fig.4 | | | | | | |
| $V_{OL}$ | LOW-level output voltage | | – | – | 0.4 | V |
| $V_{OH}$ | HIGH-level output voltage | | $0.85V_{DDD}$ | – | – | V |
| $f_{xtal}$ | crystal frequency | ±100 ppm | – | 8.4672 | – | MHz |
| $g_m$ | mutual conductance at start-up | | 19.1 | – | 23.0 | mA/V |

**Notes**

1. Assumes use of external components as shown in the application diagram; see Fig.38.
2. $R_L$ = 10 kΩ.
3. $R_L$ = 1 kΩ.
4. The typical value is as follows: $\frac{1.65 \times 3.3}{V_{DDA}}$
5. The typical value is as follows: $\frac{2.5 \times 3.3}{V_{DDA}}$
6. Pull-up/down devices are protected by a pass-gate and do not behave as a normal resistor for external applications
7. Pull-up/down resistors are connected to external power supply ($V_{DDE}$/GND).
8. Minimum condition for $V_i$ = 4.5 V, maximum condition for $V_i$ = 5.5 V.
9. Accounts for 100 mV voltage drop in both supply lines.
10. Minimum condition for $V_{TOL}$ = 4.5 V, maximum condition for $V_{TOL}$ = 5.5 V.
11. Leakage path from pad to ground.

## 11 OPERATING CHARACTERISTICS (SUBCODE INTERFACE TIMING)

$V_{DDD}$ = 1.65 to 1.95 V; $V_{SS}$ = 0 V; $T_{amb}$ = 0 to 70 °C; unless otherwise specified.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| **Subcode interface timing (single speed × n);** see Fig.34; note 1 | | | | | | |
| INPUT: PIN RCK | | | | | | |
| $t_{CLKH}$ | input clock HIGH time | | 2/n | 4/n | 6/n | µs |
| $t_{CLKL}$ | input clock LOW time | | 2/n | 4/n | 6/n | µs |
| $t_r$ | input clock rise time | | – | – | 80/n | ns |
| $t_f$ | input clock fall time | | – | – | 80/n | ns |
| $t_{d(SFSY-RCK)}$ | delay time SFSY to RCK | | 10/n | – | 20/n | µs |
| OUTPUTS: PINS SBSY, SFSY AND SUB ($C_L$ = 20 pF) | | | | | | |
| $T_{cy(block)}$ | block cycle time | | 12.0/n | 13.3/n | 14.7/n | ms |
| $t_{W(SBSY)}$ | SBSY pulse width | | – | – | 300/n | µs |
| $T_{cy(frame)}$ | frame cycle time | | 122/n | 136/n | 150/n | µs |
| $t_{W(SFSY)}$ | SFSY pulse width | 3-wire mode | – | – | 366/n | µs |
| $t_{SFSYH}$ | SFSY HIGH time | | – | – | 66/n | µs |
| $t_{SFSYL}$ | SFSY LOW time | | – | – | 84/n | µs |
| $t_{d(SFSY-SUB)}$ | delay time SFSY to SUB (P data) valid | | – | – | 1/n | µs |
| $t_{d(RCK-SUB)}$ | delay time RCK falling to SUB | | – | – | 0 | µs |
| $t_{h(RCK-SUB)}$ | hold time RCK to SUB | | – | – | 0.7/n | µs |

**Note**

1. In the normal operating mode the subcode timing is directly related to the overspeed factor ‘n’. In the lock-to-disc mode ‘n’ is replaced by the disc speed factor ‘d’,

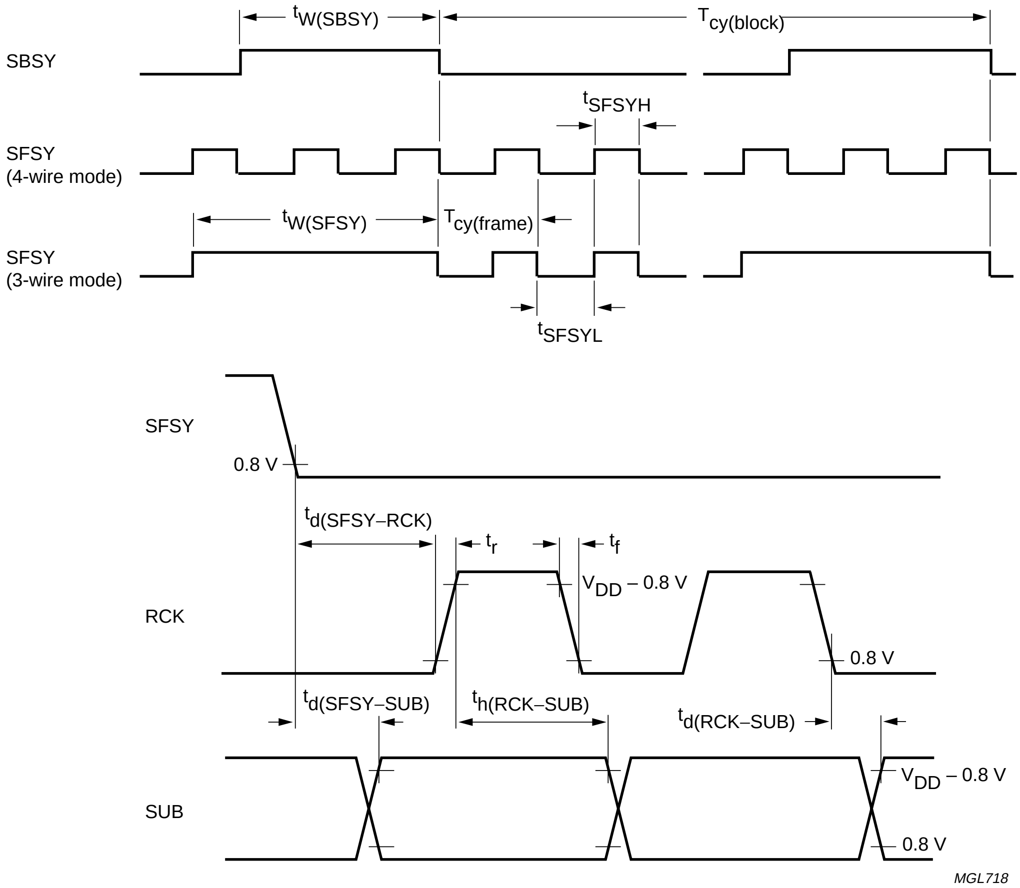



Fig.34 Subcode interface timing diagram.

## 12 OPERATING CHARACTERISTICS ($I^2S$-BUS TIMING)

$V_{DDD}$ = 1.65 to 1.95 V; $V_{SS}$ = 0 V; $T_{amb}$ = 0 to 70 °C; unless otherwise specified.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| **$I^2S$-bus timing (single speed × n);** see Fig.35; note 1 | | | | | | |
| CLOCK OUTPUT: PIN SCLK ($C_L$ = 20 pF) | | | | | | |
| $T_{cy}$ | output clock period | sample rate = $f_s$ | – | 472.4/n | – | ns |
| | | sample rate = $2f_s$ | – | 236.2/n | – | ns |
| | | sample rate = $4f_s$ | – | 118.1/n | – | ns |
| $t_{CH}$ | clock HIGH time | sample rate = $f_s$ | 166/n | – | – | ns |
| | | sample rate = $2f_s$ | 83/n | – | – | ns |
| | | sample rate = $4f_s$ | 42/n | – | – | ns |
| $t_{CL}$ | clock LOW time | sample rate = $f_s$ | 166/n | – | – | ns |
| | | sample rate = $2f_s$ | 83/n | – | – | ns |
| | | sample rate = $4f_s$ | 42/n | – | – | ns |
| OUTPUTS: PINS WCLK, DATA AND EF ($C_L$ = 20 pF) | | | | | | |
| $t_{su}$ | set-up time | sample rate = $f_s$ | 95/n | – | – | ns |
| | | sample rate = $2f_s$ | 48/n | – | – | ns |
| | | sample rate = $4f_s$ | 24/n | – | – | ns |
| $t_h$ | hold time | sample rate = $f_s$ | 95/n | – | – | ns |
| | | sample rate = $2f_s$ | 48/n | – | – | ns |
| | | sample rate = $4f_s$ | 24/n | – | – | ns |

**Note**

1. In the normal operating mode the $I^2S$-bus timing is directly related to the overspeed factor ‘n’. In the lock-to-disc mode ‘n’ is replaced by the disc speed factor ‘d’.

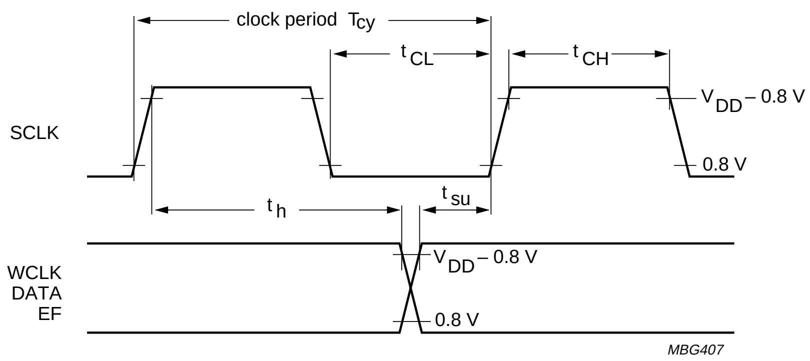



Fig.35 $I^2S$-bus timing diagram.

## 13 OPERATING CHARACTERISTICS (MICROCONTROLLER INTERFACE TIMING)

$V_{DD}$ = 1.65 to 1.95 V; $V_{SS}$ = 0 V; $T_{amb}$ = 0 to 70 °C; unless otherwise specified.

| SYMBOL | PARAMETER | CONDITIONS | NORMAL MODE | | LOCK-TO-DISC MODE | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | |
| **Microcontroller interface timing (4-wire bus mode; writing to decoder registers 0 to F; reading Q-channel subcode and decoder status);** see Figs.36 and 37; note 1 | | | | | | | |
| INPUTS SCL AND RAB | | | | | | | |
| $t_{CL}$ | input clock LOW time | | 480/n + 20 | – | 2400/n + 20 | – | ns |
| $t_{CH}$ | input clock HIGH time | | 480/n + 20 | – | 2400/n + 20 | – | ns |
| $t_r$ | input rise time | | – | 480/n | – | 480/n | ns |
| $t_f$ | input fall time | | – | 480/n | – | 480/n | ns |
| READ MODE ($C_L$ = 20 pF) | | | | | | | |
| $t_{dRD}$ | delay time RAB to SDA valid | | – | 50 | – | 50 | ns |
| $t_{PD}$ | propagation delay SCL to SDA | | 720/n – 20 | 960/n + 20 | 720/n + 20 | 4800/n + 20 | |
| $t_{dRZ}$ | delay time RAB to SDA high-impedance | | – | 50 | – | 50 | ns |
| WRITE MODE ($C_L$ = 20 pF) | | | | | | | |
| $t_{suD}$ | set-up time SDA to SCL | note 2 | 20 – 720/n | – | 20 – 720/n | – | ns |
| $t_{hD}$ | hold time SCL to SDA | | – | 960/n + 20 | – | 4800/n + 20 | ns |
| $t_{suCR}$ | set-up time SCL to RAB | | 240/n + 20 | – | 1200/n + 20 | – | ns |
| $t_{dWZ}$ | delay time SDA to RAB high-impedance | | 0 | – | 0 | – | ns |
| **Microcontroller interface timing (4-wire bus mode; servo commands);** see Figs.36 and 38; note 2 | | | | | | | |
| INPUTS SCL AND SILD | | | | | | | |
| $t_L$ | input LOW time | | 710 | – | 710 | – | ns |
| $t_H$ | input HIGH time | | 710 | – | 710 | – | ns |
| $t_r$ | input rise time | | – | 240 | – | 240 | ns |
| $t_f$ | input fall time | | – | 240 | – | 240 | ns |
| READ MODE ($C_L$ = 20 pF) | | | | | | | |
| $t_{dLD}$ | delay time SILD to SDA valid | | – | 25 | – | 25 | ns |
| $t_{PD}$ | propagation delay SCL to SDA | | – | 950 | – | 950 | ns |
| $t_{dLZ}$ | delay time SILD to SDA high-impedance | | – | 50 | – | 50 | ns |
| $t_{suCLR}$ | set-up time SCL to SILD | | 480 | – | 480 | – | ns |

| SYMBOL | PARAMETER | CONDITIONS | NORMAL MODE | | LOCK-TO-DISC MODE | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | |
| $t_{hCLR}$ | hold time SILD to SCL | | 830 | – | 830 | – | ns |
| WRITE MODE ($C_L$ = 20 pF) | | | | | | | |
| $t_{sD}$ | set-up time SDA to SCL | | 0 | – | 0 | – | ns |
| $t_{hD}$ | hold time SCL to SDA | | 950 | – | 950 | – | ns |
| $t_{sCL}$ | set-up time SCL to SILD | | 480 | – | 480 | – | ns |
| $t_{hCL}$ | hold time SILD to SCL | | 120 | – | 120 | – | ns |
| $t_{dPLP}$ | delay between two SILD pulses | | 70 | – | 70 | – | ns |
| $t_{dWZ}$ | delay time SDA to SILD high-impedance | | 0 | – | 0 | – | ns |

**Notes**

1. The 4-wire bus mode microcontroller interface timing for writing to decoder registers 0 to F, and reading Q-channel subcode and decoder status, is a function of the overspeed factor ‘n’. In the lock-to-disc mode the maximum data rate is lower.
2. Negative set-up time means that the data may change after clock transition.

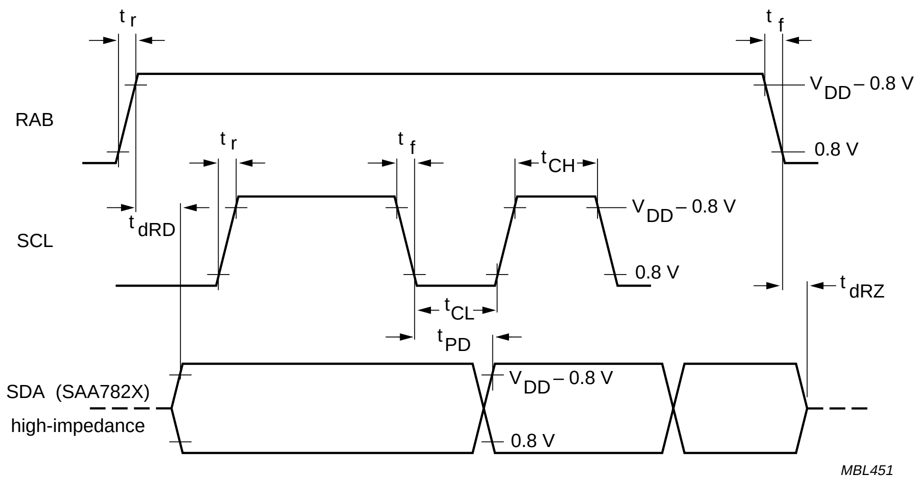



Fig.36 4-wire microcontroller timing; read mode (Q-channel subcode and decoder status information).

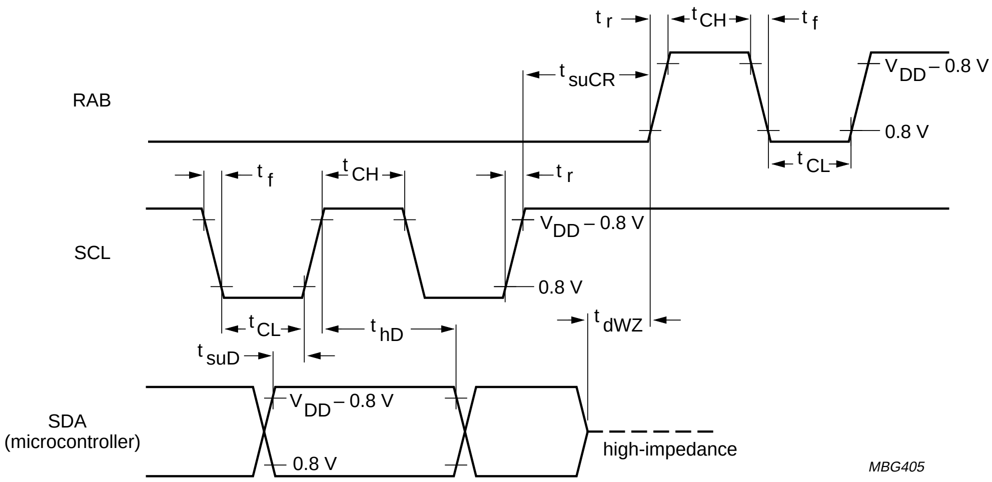



Fig.37 4-wire bus microcontroller timing; write mode (decoder registers 0 to F).

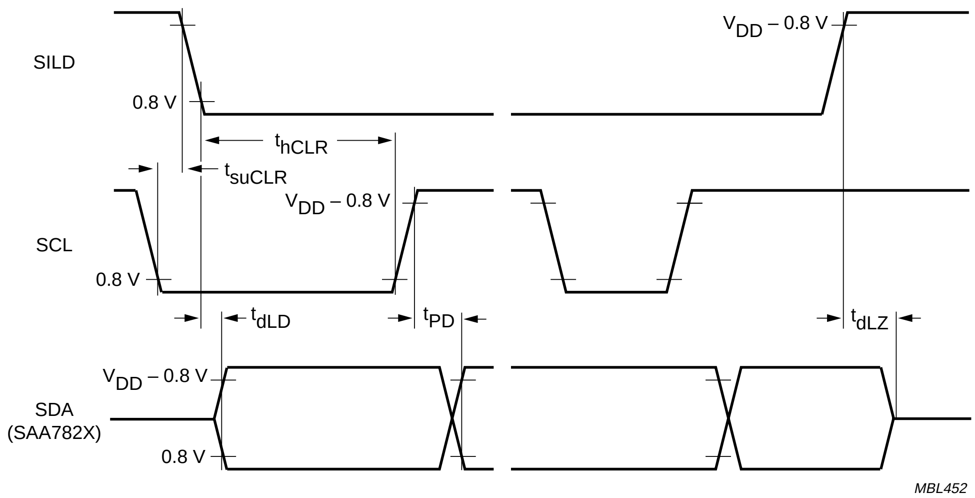



Fig.38 4-wire bus microcontroller timing; read mode (servo commands).

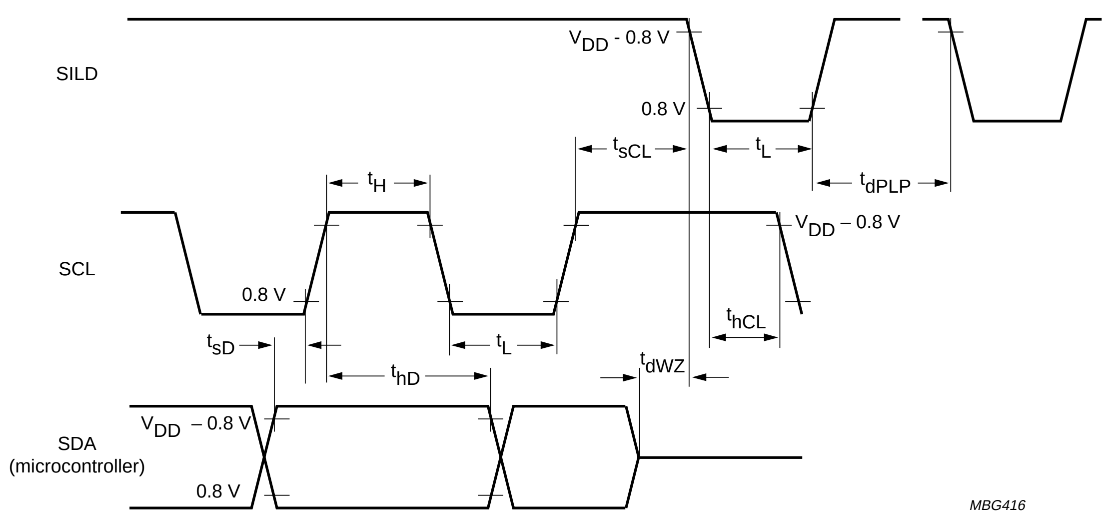



Fig.39 4-wire bus microcontroller timing; write mode (servo commands).

## 14 APPLICATION INFORMATION

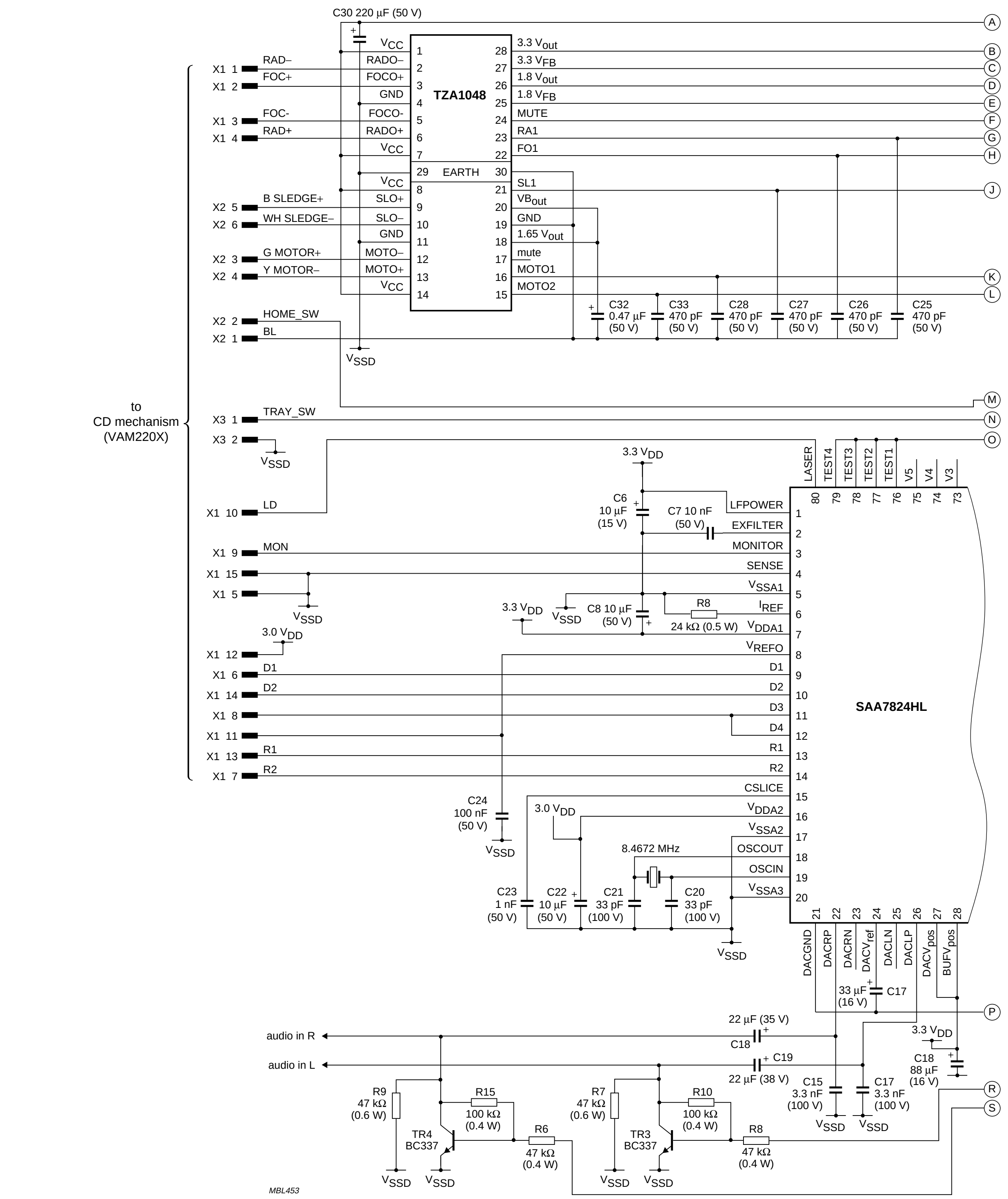



Fig.40 Typical application diagram incorporating a voltage mechanism (continued in Fig.41).

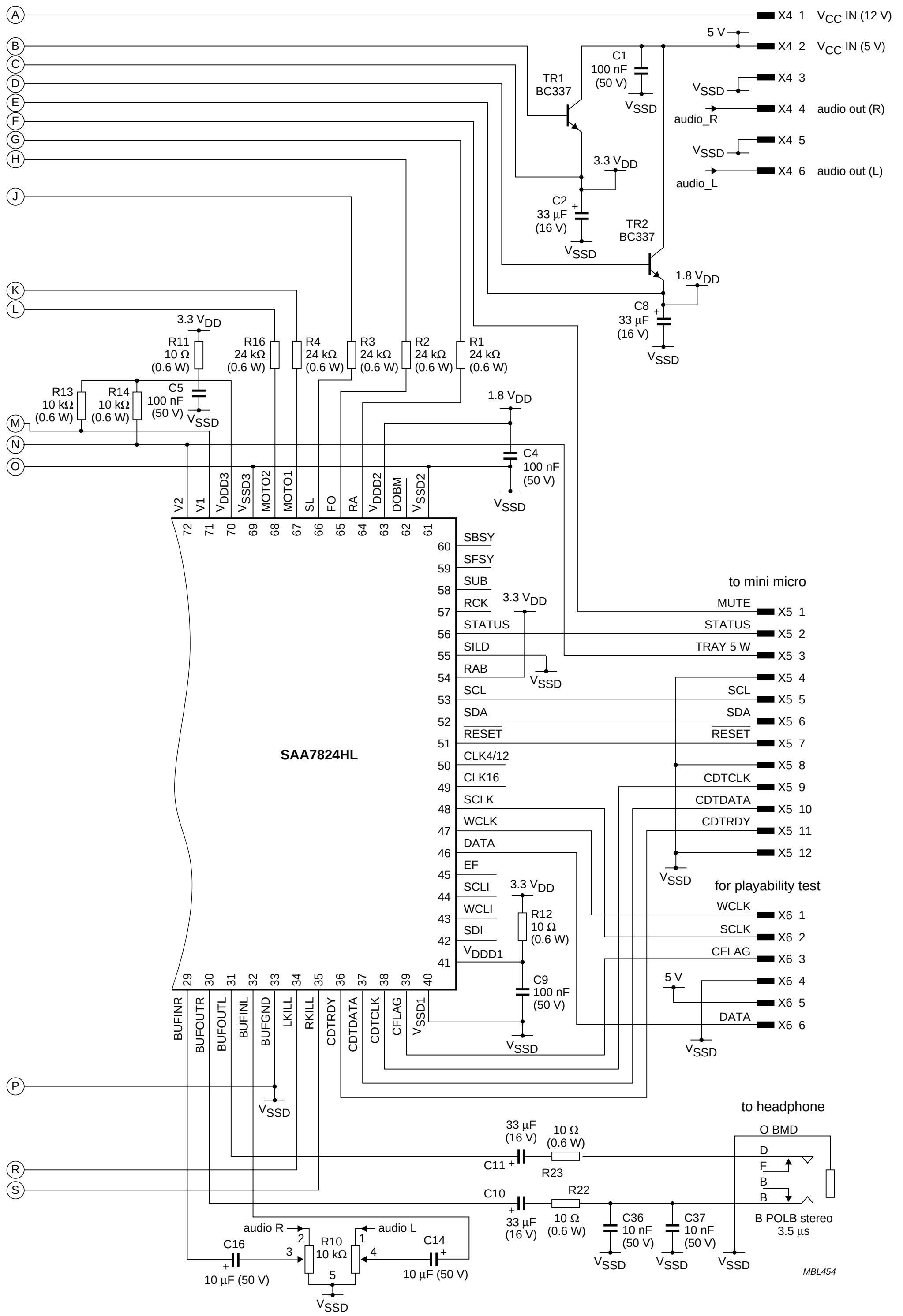
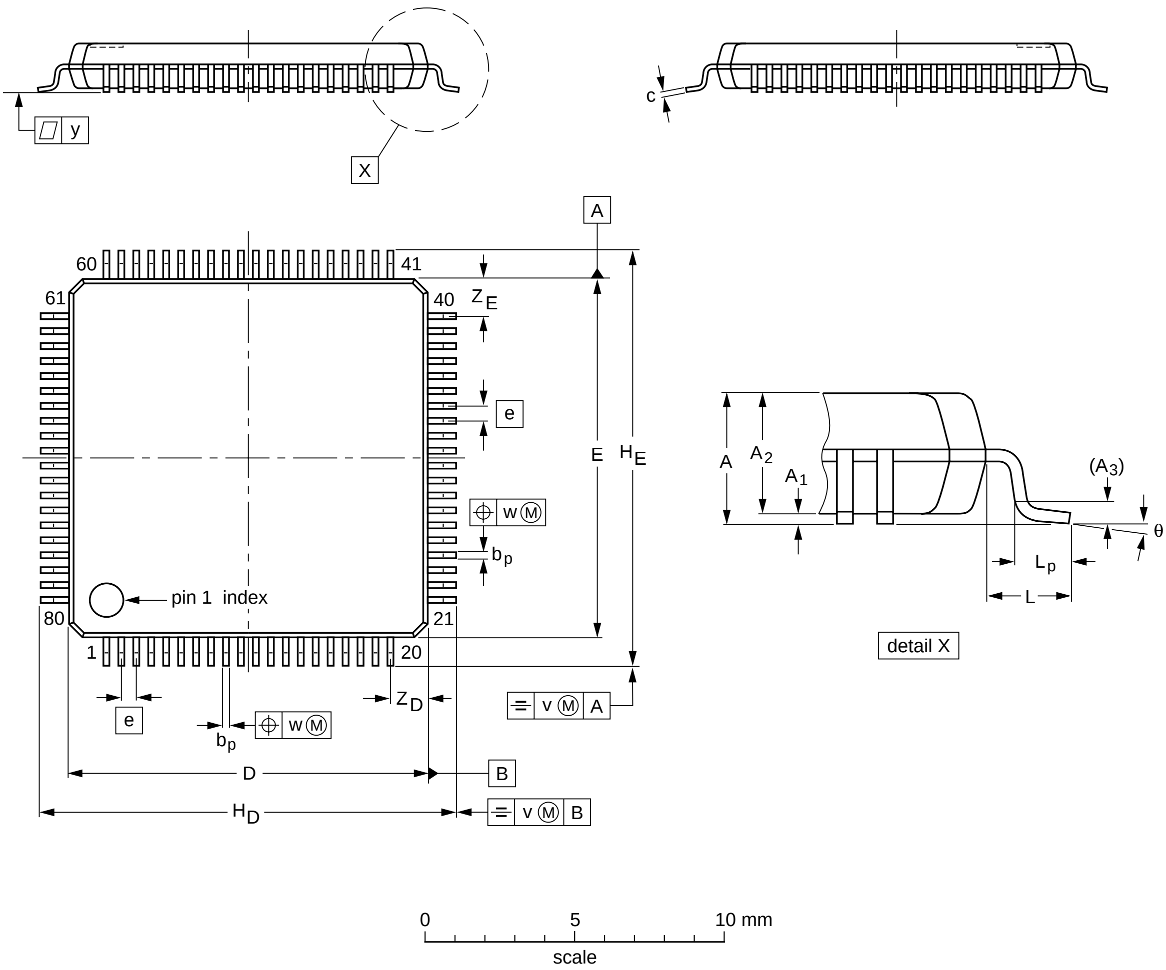



Fig.41 Typical application diagram incorporating a voltage mechanism (continued from Fig.40).

## 15 PACKAGE OUTLINE

**LQFP80: plastic low profile quad flat package; 80 leads; body 12 x 12 x 1.4 mm** **SOT315-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(1)}$ | e | $H_D$ | $H_E$ | L | $L_p$ | v | w | y | $Z_D^{(1)}$ | $Z_E^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.6 | 0.16<br>0.04 | 1.5<br>1.3 | 0.25 | 0.27<br>0.13 | 0.18<br>0.12 | 12.1<br>11.9 | 12.1<br>11.9 | 0.5 | 14.15<br>13.85 | 14.15<br>13.85 | 1 | 0.75<br>0.30 | 0.2 | 0.15 | 0.1 | 1.45<br>1.05 | 1.45<br>1.05 | 7°<br>0° |

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT315-1 | 136E15 | MS-026 | | | | ~~00-01-19~~<br>03-02-25 |

## 16 SOLDERING

### 16.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

### 16.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

### 16.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

### 16.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

### 16.5 Suitability of surface mount IC packages for wave and reflow soldering methods

| PACKAGE[1] | SOLDERING METHOD | |
|---|---|---|
| | WAVE | REFLOW[2] |
| BGA, LBGA, LFBGA, SQFP, TFBGA, VFBGA | not suitable | suitable |
| HBCC, HBGA, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, HVSON, SMS | not suitable[3] | suitable |
| PLCC[4], SO, SOJ | suitable | suitable |
| LQFP, QFP, TQFP | not recommended[4][5] | suitable |
| SSOP, TSSOP, VSO | not recommended[6] | suitable |

**Notes**

1. For more detailed information on the BGA packages refer to the *"(LF)BGA Application Note"* (AN01026); order a copy from your Philips Semiconductors sales office.
2. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
3. These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
4. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
5. Wave soldering is suitable for LQFP, TQFP and QFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
6. Wave soldering is suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

## 17 DATA SHEET STATUS

| LEVEL | DATA SHEET STATUS(1) | PRODUCT STATUS(2)(3) | DEFINITION |
|---|---|---|---|
| I | Objective data | Development | This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice. |
| II | Preliminary data | Qualification | This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product. |
| III | Product data | Production | This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN). |

**Notes**

1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.
3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

## 18 DEFINITIONS

**Short-form specification** — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

**Application information** — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

## 19 DISCLAIMERS

**Life support applications** — These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Semiconductors customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors for any damages resulting from such application.

**Right to make changes** — Philips Semiconductors reserves the right to make changes in the products - including circuits, standard cells, and/or software - described or contained herein in order to improve design and/or performance. When the product is in full production (status ‘Production’), relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN). Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no licence or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified.

## 20 PURCHASE OF PHILIPS I$^2$C COMPONENTS

# *Philips Semiconductors – a worldwide company*

**Contact information**

For additional information please visit **http://www.semiconductors.philips.com**. Fax: **+31 40 27 24825**
For sales offices addresses send e-mail to: **sales.addresses@www.semiconductors.philips.com**.



SCA75



Printed in The Netherlands R04/03/pp89 Date of release: 2003 Oct 01 Document order number: 9397 750 12009